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COMMUNICATIONS

Of The Association For

COMPUTING MACHINERY

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COMMUNICATIONS OF THE ASSOCIATION FOR COMPUTING MACHINERY

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OFFICIAL NOTICES

1958 EASTERN JOINT COMPUTER CONFERENCE

December 3-5, 1958

Bellevue-Stratford Hotel, Philadelphia, Pa.

PRELIMINARY TECHNICAL PROGRAM

TUESDAY, DECEMBER 2

7:00 p.m.- 9:00 p.m. Registration Opens

WEDNESDAY, DECEMBER 3

8:00 a.m.-10:00 a.m. Registration

OPENING SESSION

10:00 a.m.-12:00 noon

Chairman: F. M. Verzuh, Massachusetts Institute of Technology

Wednesday, December 3, 1958

SESSION II

2:00 p.m.- 5:00 p.m.

Wednesday, December 3, 1958

RELIABILITY AND COMPONENTS

Chairman: N. P. Edwards, International Business Machines Corporation

PART A. RELIABILITY OF DATA PROCESSING EQUIPMENT

ATHENA COMPUTER: A RELIABILITY REPORT

Speakers: G. A. Raymond and L. W. Reid, Remington Rand

PHILOSOPHY OF AUTOMATIC ERROR CORRECTION

Speaker: R. M. Block, Datamatic Division of Minneapolis-Honeywell

THE SYSTEMS APPROACH TO RELIABILITY

Speaker: H. D. Ross, International Business Machines Corporation

PART B. MODERN COMPUTER COMPONENTS

IMPULSE SWITCHING OF FERRITES

Speaker: R. E. McMahon, Massachusetts Institute of Technology, Lincoln Lab.

A HIGH SPEED, HIGH CAPACITY PHOTO MEMORY

Speaker: C. A. Lovell, Bell Telephone Laboratories

DESIGN CRITERIA FOR LONG-WEARING COMPUTER TAPE

Speaker: J. W. Wenner, International Business Machines Corporation

SESSION III

9:00 a.m.-12:00 noon

Thursday, December 4, 1958

THE IMPENDING REVOLUTION IN COMPUTER TECHNOLOGY

Chairman: Rex Rice, I B M. Research Center, Poughkeepsie, New York

PART A—STATUS OF PRESENT RESEARCH

INTRODUCTION

Speaker: R. Rice, I.B.M. Research Center, Poughkeepsie, New York

COMPUTER DESIGN FROM THE PROGRAMMER'S VIEWPOINT

Speaker: Walter F. Bauer, Space Technology Laboratory, Ramo-Wooldridge Corp.

DEVICE, CIRCUIT AND LOGICAL ELEMENT TRENDS
Speaker: Dudley Buck, Massachusetts Institute of Technology

NEW SYSTEM DESIGN TECHNIQUES
Speaker: R. K. Richards, Consultant

PART B—SPECULATION ON FUTURE

Should we abandon the general purpose coding and machine concepts?

Programming Perspectives	W. F. Bauer
System Design	R. K. Richards
Devices Leading to Self Organizing Systems	Dudley Buck

SESSION IV

2:00 p.m.— 5:00 p.m.

Thursday, December 4, 1958

ORGANIZATION AND PROCESSING OF INFORMATION

Chairman: W. Orchard-Hays, Corporation for Economic and Industrial Research

PART A. ORGANIZATIONAL AND PROGRAMMING METHODS

AN INFORMATION FILING AND RETRIEVAL SYSTEM FOR THE ENGINEERING AND MANAGEMENT RECORDS OF A LARGE-SCALE COMPUTER DEVELOPMENT PROJECT

Speakers: G. A. Bernard III and Louis Fein, Ampex Corporation

FILE PROBLEMS CONNECTED WITH A NATIONAL MENU STUDY

Speaker: Phil M. Thompson, Market Research Corporation of America

DATA PROCESSING AND INFORMATION PRODUCTION

Speakers: Robert H. Gregory and Martin Trust, Massachusetts Institute of Technology

INTERMISSION

PART B. HARDWARE AND SYSTEMS METHODS

NBS MULTI-COMPUTER SYSTEM

Speakers: A. L. Leiner, W. A. Notz, J. L. Smith and A. Weinberger, National Bureau of Standards

DATA HANDLING BY CONTROL WORDS

Speaker: G. A. Blaauw, International Business Machines Corporation

SESSION V

2:00 p.m.— 5:00 p.m.

(Parallel Session)

Thursday, December 4, 1958

DESIGN TECHNIQUES

Chairman: F. H. Tendick, Bell Telephone Laboratories

SPECIAL PURPOSE COMPUTER DESIGN BY SIMULATION

Speaker: P. L. Phipps, Remington Rand Univac, St. Paul

LOGICAL DESIGN TECHNIQUES FOR CG-24 A GENERAL PURPOSE REAL TIME COMPUTER

Speakers: G. P. Dineen, I. L. Lebow and I. S. Reed, Massachusetts Institute of Technology, Lincoln Laboratory

DESIGN CRITERIA FOR AUTOSYNCHRONOUS CIRCUITS

Speakers: J. C. Sims, Jr., Sylvania Electric Products, Inc., and
H. J. Gray, University of Pennsylvania

ANALYSIS OF TRL CIRCUIT PROPAGATION DELAY

Speakers: W. J. Dunnet, E. P. Auger and A. C. Scott, Sylvania Electric Products, Inc.

THE RECORDING, CHECKING AND AUTOMATIC PRINTING OF TRANSISTOR LOGICAL DIAGRAMS

Speakers: P. W. Case and M. Kloomok, International Business Machines Corporation

SESSION VI

9:00 a.m.-12:00 noon

Friday, December 5, 1958

SPECIAL APPLICATIONS

Chairman: E. L. Harder, Westinghouse Electric Corp., Pittsburgh, Pa.

SYSTEM EVALUATION AND INSTRUMENTATION USING SIMULATION EQUIPMENT

Speakers: A. J. Strassman & L. H. Kurkjian, Hughes Aircraft Co., Fullerton, Cal.

AUTOMATIC PROGRAMMING SYSTEM FOR TRANSLATION OF RUSSIAN TO ENGLISH

Speaker: V. E. Giuliano, Harvard Computation Laboratory, Cambridge

APAR—AUTOMATIC PROGRAMMING AND RECORDING

Speakers: G. R. Bachand, J. L. Rogers, T. F. Marker, Sandia Corp., New Mexico

DYANA—DYNAMICS ANALYZER-PROGRAMMER

Speaker: T. J. Theodoroff, General Motors Corp., Detroit

UNIVAC AIR LINES RESERVATIONS SYSTEMS

Speakers: C. W. Fritze, V. E. Herzfeld, D. K. Sampson, Remington Rand Univac, St. Paul

SESSION VII

2:00 p.m.- 5:00 p.m.

Friday, December 5, 1958

NEW COMPUTERS

Chairman: T. H. Bonn, Remington Rand Univac, Philadelphia, Pa.

THE SIEMENS DIGITAL COMPUTER—2002

Speaker: Dr. Heinz Guzin, Siemens & Halske, A. G., Munich, Germany

DESIGN OF THE RCA 501 SYSTEM

Speakers: T. M. Hurewitz and J. G. Smith, Radio Corporation of America

THE IBM 7070—DATA PROCESSING SYSTEM

Speakers: R. W. Avery, S. H. Blackford and J. McDonnell, International Business Machines Corporation

PERFORMANCE ADVANCES IN A TRANSISTORIZED COMPUTER SYSTEM, THE TRANSAC S-2000

Speakers: R. J. Segal, J. L. Maddox and P. Plano, Phileo Corporation

PROGRAMMING DESIGN FEATURES OF GAMMA 60 COMPUTER

Speaker: Philippe Dreyfus, Cie Des Machines Bull, Paris, France

TECHNIQUES DEPARTMENT

Dear Bob:

This letter is being sent to you both as Techniques Editor of the *Communications* and as an interested party. I found the POL-UNCOL-ML report in the August issue very interesting since we have arrived at just about the same conclusions. Furthermore I have developed an UNCOL, a version of which we will use when we put the RUNCIBLE successor on the Univac. The enclosed paper describes the language in the jargon of the August report.

The similarity of the language with Polish notation has led us to begin a rigorous characterization of it. It seems that one might fruitfully define transformations on strings in the language to optimize a space-time functional for a given machine (e.g., the "653 function" which will tolerate a few more instructions here and there if the result is less execution time through greater use of the core storage).

I submit the paper for publication and for your comments.

Sincerely,
Mel

PROPOSAL FOR AN UNCOL

MELVIN E. CONWAY, Case Institute of Technology

This discussion contains a proposal for a universal computer-oriented language (UNCOL) to be used as a common path between the problem-oriented language (POL) and the machine language (ML) in compatible automatic programming systems. (See Ref. 1.)

The totality of desired characteristics of a useful UNCOL cannot be completely known because of the possible emergence of a machine whose programming method is basically different from those currently used, but at the present time at least, a computer-oriented language is one which describes a computation in terms of a sequence of operations, each of which operates on information stored in machine registers or alters the sequence of operations.

The language described herein has been motivated by practical considerations in the programming of RUNCIBLE², an existing IT-to-650 compiler, for the Univac 1. The memory size of the Univac 1, on which the compilation will take place, demands that there be at least one intermediate language which can be stored on tape during the compilation process. Experimentation with several intermediate languages has indicated that the one which provides the greatest opportunities for subsequent economization of machine code resembles the code of a single-address computer, and the simpler this computer (i.e., the fewer the registers and instructions available) the greater are the opportunities to translate this intermediate code into tight machine code. This happy fact implies that universality of the intermediate language (in the sense that it is not biased toward any computer) goes hand-in-hand with efficiency of the resultant machine code. Therefore the proper design of an UNCOL will not only aid intercommunication among machines but will result in the production of better programs.

The technique of programming in this UNCOL, which I shall call SML (simple machine language), is to reduce a computation to a sequence of minimal arithmetic or logical operations, to transfer the arguments of each operation to standard storage positions, and to express each operation as a subroutine linkage ("execute"). There are only two instructions in SML, a memory-to-memory transfer and an execute instruction.

Programs refer to four types of memory: general (G-) storage, temporary (T-) storage, argument (A-) storage, and result (R-) storage. These are distinguished by the roles they play in the computation.

Variables which appear in the POL and constants are held in G-storage. Hence the operation $Y \leftarrow (B*C) + D$ finds B, C, and D in G-storage and stores the result Y there.

Intermediate results in a given calculation which have not been given a name in the POL are stored in T-storage. For example, if the sequence of $Y \leftarrow (B*C) + (D*E)$ is

1. Execute $B*C$
2. Store the result
3. Execute $D*E$
4. Execute the addition
5. Store the result in Y ,

then the store operation of step 2 will be into T-storage.

A-storage holds the operands (arguments) of all operations. Hence "execute $B*C$ " assumes that B and C have been put into A-storage.

The result of every manipulative operation (as distinguished from a comparison operation which has no "result") is found in R-storage. Although existing POLs do not demand it the possibility of multiple output operations is included in the language.

Each operation is preceded by the memory-to-memory transfers necessary to load A-storage and succeeded by the memory-to-memory transfers necessary to empty R-storage. The storage registers (except for G-storage) are denoted by the Roman letters T, A, or R subscripted by a non-negative integer. In SML a memory-to-memory transfer is represented by a pair of memory locations. For example, (T_0, A_1) means "read out of T_0 into A_1 " or " $T_0 \rightarrow A_1$ " and is conventionally coded as "load T_0 , store A_1 ".

Addresses in G-storage are given any name desired except, of course, for names like T_0 and A_1 . If appropriate, these names will be taken from the POL-coding. In addition there is a class of G-addresses denoted by a star (*) whose name indicates the contents of the memory location. For example, $(*1.0, A_1)$ means "read a floating-point 1 into A_1 ". Starred G-addresses may appear as the left member only of a transfer pair.

An operation is denoted by the letter "X" (execute) followed by parentheses enclosing the name of the operation: $X((A_0)*(A_1) \rightarrow R_0)$, floating point). In order to reduce the number of possible operations there are conventions on the use of A- and R-storage. The n arguments of an n-ary operator will be placed into the set (A_0, \dots, A_{n-1}) and the correspondence is specified by the usual order in which the arguments of the operator are written. The results are similarly lined up in R-storage. For example the numerator of a divide goes into A_0 and the denominator goes into A_1 . With these conventions the above example is equivalent to $X(\text{floating point } *)$.

Some readers may have been disturbed by the fact that the allocation of G- vs. T-storage depends on the POL. The simplification rule stated below removes part of the objectionableness of this practice, in that superfluous temporary storage not mentioned in the POL will not appear in the UNCOL. The other half of the problem is more difficult and indeed arises whenever one tries to describe a given computation equivalently in two different languages: since many POLs may specify too much temporary storage (e.g., any three-address system, or even a Fortran-type language with too-finely-divided statements) how can this inefficiency be kept from getting into the UNCOL? The answers to this question are to be found partially in the design of the POL and partly in the algorithms of the POL-to-UNCOL generator, which should perform the currently avoided task of scanning a program as a whole for redundancies.

Certain seemingly obvious simplifications of SML must be avoided, whereas others are acceptable. The criterion for acceptability of a simplification rule rests on the way it will complicate the algorithms for conversion of SML into ML. For example, if $Y \leftarrow (B*C) + D$ is scanned from the right the corresponding SML program is

(D, T_0)
 (C, A_1)
 (B, A_0)
 $X(*)$
 (R_0, A_0)
 (T_0, A_1)
 $X(+)$
 (R_0, Y) .

One acceptable simplification rule eliminates all transfers of the form $(G\text{-address}, T_k)$ by replacing the subsequent (T_k, A_n) by $(G\text{-address}, A_n)$. In our example the SML program resulting from such a simplification is

(C, A₁)
(B, A₀)
X(*)
(R₀, A₀)
(D, A₁)
X(+)
(R₀, Y).

The following example illustrates that using the above rule for R-address (rather than G-address) would be an unacceptable simplification:

Y ← |B| + |C| should generate

(C, A₀)
X(magnitude)
(R₀, T₀)
(B, A₀)
X(magnitude)
(R₀, A₀)
(T₀, A₁)
X(+)
(R₀, Y).

The sequence

(C, A₀)
X(magnitude)
(R₀, A₁)
(B, A₀)
X(magnitude)
(R₀, A₀)
X(+)
(R₀, Y) is incorrect for two reasons:

1. on a given object machine A₁ may be a register which is destroyed by the magnitude operation, and
2. the algorithms for translation from SML to ML are greatly simplified by the assumption that preceding each n-ary operation there will be precisely n transfers of the form (−, A_k); (k = 0, ..., n − 1). Such mistakes can be avoided by adopting the rule that A- and R-storage are not usable across an operation.

So far we have discussed only replacement statements (equations). SML must contain several other types of information. Somewhere (probably at the beginning to simplify the job of the SML-ML translator) there should be a list of storage requirements for arrays. Certain points in the SML program should be tagged (just as statements have their numbers) and the tag should carry information as to whether or not it will be used as an entrance point into the instruction sequence. Finally, there are certain operations of the "jump" type: "jump to the point in the program whose tag is in A₀ (if A₁ = A₂)". The quantity in A₀ may be the result of a calculation or it may be a name which was carried over from the POL. In the latter case there may be good reason not to carry around the statement names in the ML program: the SML-ML translator will have to make such decisions. There are other operations all of whose arguments may not appear explicitly in the ML program; "get the doubly-subscripted variable whose name is in A₀, whose matrix width is in A₁, and whose subscripts are in A₂ and A₃, such that the subscripts of the upper-left-hand element are in A₄ and A₅"; "get the next item in the serial input file whose name is in A₀". The latter implies the existence of some file designs at the beginning of the program. When a name is put into A-storage it comes via a transfer from starred G-storage: (*input file 3, A₀). Thus the translator can go back in the instruction list and find out the name.

The methods used to turn the POL into SML of course depend on the input, but this much can be said: because of the regularity of SML the job will be simpler than that of turning our symbolic coding for an existing machine.

More can be said about the SML-ML translator. The way we are programming RUNCIBLE for the Univac, the translator will consist of two parts: 1) SML to inefficient ML; 2) inefficient ML to good ML. (ML here means symbolic ML, UNISAP^s.) The "inefficient ML" will work but will be wasteful of space. The chief job of part 1 is to decide what operations can be done by the hardware and do not require a reference to the library, and to translate, for each operation, A- and R-storage into appropriate machine registers. Part 2 keeps a table of the contents of the machine equivalents of A-, R-, and T-storage and weeds out about as much coding as a human programmer could, subject to the restriction that he may not permute operations.

I have tried to describe in rough terms an UNCOL, whose suitability for describing arithmetic computation will be ascertained in our current flow-charting of a compiler which uses it. The suitability of SML for all computation is open to question, but assuming some kind of communication (regarding what are legitimate operations) between the POL-SML phase and the SML-ML phase, the complete generality of SML is very plausible.

Notes

1. Share Ad-Hoc Committee on Universal Languages, *The Problem of Programming Communication With Changing Machines*, Communications of the ACM, Vol. 1, No. 8, August 1958.
2. Computing Center Staff, *RUNCIBLE 1*, Computing Center No. 1008, Case Institute of Technology, August 1958.
3. Conway, M. E., *UNISAP*, Computing Center No. 1009, Case Institute of Technology, August 1958.

ON THE EQUIVALENCE AND TRANSFORMATION OF PROGRAM SCHEMES

IU. I. IANOV

Doklady, AN USSR, vol. 113, No. 1, 1957, pp. 39-42
Translated by MORRIS D. FRIEDMAN, Lincoln Laboratory

Editor's Note: This is a translation of the first of two related Russian articles. The second article will be published in a later issue of the COMMUNICATIONS.

When programming for universal automatic computers, (logical) program schemes (PS) are used [1]. Inasmuch as a PS is not determined uniquely by an algorithm, questions of the equivalence and also of the identical transformation of the PS arise. In this note, the PS are considered as specific listings of the order of completion of the operators and of the logical conditions depending on the values of the logical (binary) variables.* Hence, the operators are considered as elementary objects to which a specific capacity to alter the values of the logical variables is attributed.

DEFINITION 1. The symbols $\underline{\underline{\alpha}}_i$, $\underline{\underline{\beta}}_j$ with the natural subscripts i, j will be called the left and right strokes, respectively. We will call the ordered set of the logic-algebra function α and the left stroke $\underline{\underline{\alpha}}_i$ the logical condition α_i . We will call the operators $A_1, A_2 \dots$ and the logical conditions, elementary expressions (EE).

DEFINITION 2. The finite line composed of operator symbols A_1, A_2, \dots , logical conditions α_i, β_j, \dots and right strokes $\underline{\underline{\alpha}}_i, \underline{\underline{\beta}}_j, \dots$ such that one and only one right stroke $\underline{\underline{\alpha}}_i$ with the same subscript i is found in this line for each left stroke $\underline{\underline{\alpha}}_i$ with the subscript i which enters into this line and, conversely, one and only one left stroke with the same subscript is found for each right stroke $\underline{\underline{\alpha}}_i$, is called a program scheme.

We will consider that each entry of the operator into the PS is independent.

* Assuming the values 0 and 1, where let 0 correspond to "false" and 1 to "true".

DEFINITION 3. Let there be the PS $U(p_1, \dots, p_k, A_1, \dots, A_n)$ where p_1, \dots, p_k are independent logical variables. Let us denote all possible sets of values of the variables p_1, \dots, p_k by $\Delta_1, \dots, \Delta_{2^k}$. Let us call the value of the scheme $U(p_1, \dots, p_k, A_1, \dots, A_n)$ for the sequence of sets

$$(1) \quad \Delta_{s_1}, \Delta_{s_2}, \dots, \Delta_{s_m}, \Delta_{s_{m+1}}, \dots \quad (1 \leq s_j \leq 2^k, j=1, 2, \dots)$$

a line of operators obtained by the following process.

1st Step: Let us note the left-most symbol of the scheme U .

Let l steps be made with the result that the line of operators

$$(2) \quad A_{i_1}, A_{i_2}, \dots, A_{i_{m-1}}$$

is written (the vacant line should be denoted here by A_{i_m}). Then, let us consider the symbol marked in the l -th step in the $(l+1)$ st step, where if this is an EE then we will say that it is performed in U for the sequence (1) with the set Δ_{s_m} .

The following cases are possible:

1) The symbol noted in the l -th step is an operator. Then, we add it to the right to the line (2) and we note the symbol directly after it in the scheme U .

2) The symbol marked in the l -th step is the logical condition $\alpha(p_1, \dots, p_k)|\underline{}$. Then, if $\alpha(\Delta_{s_m}) = 1$,

let us note the symbol directly after the logical condition $\alpha|\underline{}$ in the scheme U ; if $\alpha(\Delta_{s_m}) = 0$, then

let us note the symbol standing to the right of the right stroke $|\underline{}$ in U (if such symbols occur in U).

3) Finally, if the symbol marked in the l -th step is a right stroke, then let us mark the symbol directly after it in U (if it exists). The process breaks off if no symbol has been marked at a certain step. We call the line of operators written because of this process the value of the PS U for the sequence (1). Hence, in case the process described is continued indefinitely but the line of written operators is finite, then we add to it parentheses () on the right which we will call a vacant period. We will consider the values with a vacant period infinite.

DEFINITION 4. We say that the shift distribution

$$(3) \quad A_1 - B_i \quad (i=1, \dots, n),$$

has been given for the set of operators $G = \{A_1, \dots, A_n\}$ and the set of logical variables $B = \{p_1, \dots, p_k\}$ if a certain set of logical variables $B_i \subset B$ has been placed in correspondence with each operator A_i of G .

DEFINITION 5. Let the PS $U(p_1, \dots, p_k, A_1, \dots, A_n)$ for the sequence (1) have the value

$$(4) \quad A_{i_1}, A_{i_2}, \dots, A_{i_m}, A_{i_{m+1}}, \dots$$

Then we call the sequence (1) admissible for U under the shift distribution (3) if the set $\Delta_{s_{m+1}}$ for every $m=1, 2, \dots$ differs from the set Δ_{s_m} by the values of variables only from B_{i_m} . Hence, if the line (4) is finite and A_{i_r} is its last operator then the sets $\Delta_{s_{r+2}}, \Delta_{s_{r+3}}, \dots$ are arbitrary.

DEFINITION 6. Let us say that the PS $U(p_1, \dots, p_k)$ and $B(p_1, \dots, p_k)$ are equivalent under the shift distribution (3) (which we will denote by $U=B$) if their values coincide for any sequence of sets admissible for U or B under this shift distribution.

DEFINITION 7. We say that the PS U and B are partially equivalent under the shift distribution (3) if, for any sequence of sets admissible for U or B , either their values coincide or the value of those of them for which this sequence is admissible is infinite.

The following questions are solved positively: To find the algorithm which would give an answer for any pair of PS equivalent (partially equivalent, respectively) thereto or not for a given shift distribution.

DEFINITION 8. Let us define the logic-algebra function $B_{(U)}(p_1, \dots, p_k)$ for each EE B and PS $U(p_1, \dots, p_k)$ as follows:

$$\begin{aligned} B_{(U)}^{\oplus}(\Delta_s) = & \begin{cases} 1, & \text{if } B \text{ is satisfied in } U \text{ for the stationary sequence } \Delta_s, \Delta_s, \dots, \Delta_s, \dots; \\ 0, & \text{otherwise} \end{cases} \end{aligned}$$

DEFINITION 9. We denote

$$\alpha_i^1 = \max_{B_i} \underset{\oplus}{A}_{i(U)}(p_1, \dots, p_k) \quad (i=1, \dots, n),$$

for the PS $U(p_1, \dots, p_k, A_1, \dots, A_n)$ under the shift distribution (3), where the maximum is taken over all possible sets of values of the variables from B_i and we consider the PS $U^{(1)} \equiv q_1 \vee \overline{\alpha_1^1} \mid \dots \mid_j_1$

$q_n \vee \overline{\alpha_n^1} \mid \dots \mid_j_n U(p_1, \dots, p_k, A_1 \mid \dots \mid_j_1, \dots, A_n \mid \dots \mid_j_n) \dots$ where q_1, \dots, q_n are independent logical variables.

Let the functions α_i^ν ($i=1, \dots, n$) and the PS $U^{(\nu)}$, which we will call the ν -th submergence of the PS U , be defined. Let us put

$$\alpha^{\nu+1} = \max_{B_i, q_1, \dots, q_n} \underset{\oplus}{A}_i(U^{(\nu)})(p_1, \dots, p_k, q_1, \dots, q_n) \quad (i=1, \dots, n),$$

where the maximum is taken over all possible sets of values of the variables from B_i and q_1, \dots, q_n and correspondingly

$$U^{(\nu+1)} \equiv q_1 \vee \overline{\alpha_1^{\nu+1}} \mid \dots \mid_j_1 \dots q_n \vee \overline{\alpha_n^{\nu+1}} \mid \dots \mid_j_n U(p_1, \dots, p_k, A_1 \mid \dots \mid_j_1, \dots, A_n \mid \dots \mid_j_n).$$

It is evident that** $\alpha_i^\nu \rightarrow \alpha_i^{\nu+1}$ for every $i=1, 2, \dots, n$ and $\nu=1, 2, \dots$ and, consequently, such a natural μ is found that $\alpha_i^{\mu+1} \equiv \alpha_i^\mu$ for all $i=1, 2, \dots, n$. Let us call the PS $U^{(\mu)}$, the stationary submergence of the PS U under the shift distribution (3).

DEFINITION 10. Let us call the PS $U(p_1, \dots, p_k)$ and $B(p_1, \dots, p_k)$ weakly equivalent if the first operators of their values coincide for any sequence of the form $\Delta_s, \Delta_s, \dots, \Delta_s, \dots$ where if the value of one of them is a vacant cycle or is vacant, then the value of the other PS must be the same.

THEOREM: In order that the PS $U(p_1, \dots, p_k)$ and $B(p_1, \dots, p_k)$ should be equivalent for a given shift distribution (3), it is necessary and sufficient that their stationary submergence should be weakly equivalent.

Similarly for each PS $U(p_1, \dots, p_k, A_1, \dots, A_n)$ such a system of functions $\beta_o, \beta_1, \dots, \beta_n$ can be constructed that the question of the partial equivalence of the PS of the form

$$q_o \vee \overline{\beta_o} \mid \dots \mid_j_n q_n \vee \overline{\beta_n} \mid \dots \mid_j_1 0 \mid \dots \mid_j_t U(p_1, \dots, p_k, A_1 \mid \dots \mid_j_1, \dots, A_n \mid \dots \mid_j_n).$$

The question of the identical transformations of PS reduces to the construction of a complete system of elementary transformation rules. To do this, it is first necessary to introduce the effective concept of subordination of an EE by a logical function which has the pithy meaning: if the EE B in the PS U is subordinated to the function α with the shift distribution (3), then the equality $\alpha(\Delta_s)=1$ is a necessary condition for the executability of B for the set Δ_s for any admissible sequence.

DEFINITION 11. Let us call an expression every finite line composed of various symbols of operators, logical conditions and right strokes so that not more than one left and not more than one right stroke with the subscript i is found therein for every natural number i .

Evidently an PS is an expression.

The following system of axiom schemes and derivation rules (where M, N are arbitrary expressions; $Q(M)$ is an expression containing the expression formally; A_k are arbitrary operators; $\alpha, \beta, 0, 1$ are the formulas of classical expression calculus) is complete in the sense of the deducibility of every formula of the form $U=B$ which is real for a given shift distribution, where U and B are PS.

* If U does not contain certain of the operators A_1, \dots, A_n , then the appropriate right strokes \mid_j in the construction of the PS $U^{(\nu)}$ can stand at arbitrary positions, for example, directly before U .

** That is $(\alpha_i^\nu \rightarrow \alpha_i^{\nu+1}) \equiv 1$.

I. 1) $0 \left| \begin{smallmatrix} A_k \\ i & i \end{smallmatrix} \right| = 0 \left| \begin{smallmatrix} \\ i & i \end{smallmatrix} \right| ;$

2) $1 \left| \begin{smallmatrix} M \\ i & i \end{smallmatrix} \right| = M ;$

3) $\left| \begin{smallmatrix} M 1 \\ i & i \end{smallmatrix} \right| = M .$

II. 1) $\alpha \& \beta \left| \begin{smallmatrix} M \\ i & i \end{smallmatrix} \right| = \alpha \left| \begin{smallmatrix} \beta \\ j & j \end{smallmatrix} \right| M \left| \begin{smallmatrix} \\ i & j \end{smallmatrix} \right| ;$

2) $\left| \begin{smallmatrix} M \alpha \& \beta \\ i & i & j \end{smallmatrix} \right| = \left| \begin{smallmatrix} M \alpha \\ i & j \end{smallmatrix} \right| \beta \left| \begin{smallmatrix} \\ j \end{smallmatrix} \right| ;$

3) $\alpha \vee \beta \left| \begin{smallmatrix} \\ i & j \end{smallmatrix} \right| = \bar{\alpha} \left| \begin{smallmatrix} \\ j \end{smallmatrix} \right| \beta \left| \begin{smallmatrix} \\ i & j \end{smallmatrix} \right| .$

III. $M N = 0 \left| \begin{smallmatrix} \\ i & j \end{smallmatrix} \right| N 0 \left| \begin{smallmatrix} \\ k & i \end{smallmatrix} \right| M 0 \left| \begin{smallmatrix} \\ j & k \end{smallmatrix} \right| .$

IV. $\left| \begin{smallmatrix} \\ i & j \end{smallmatrix} \right| = \left| \begin{smallmatrix} \\ j & i \end{smallmatrix} \right| .$

V. $\alpha \left| \begin{smallmatrix} \\ i & j \end{smallmatrix} \right| = \Lambda$, where Λ is a vacant scheme

VI. 1) $\alpha \left| \begin{smallmatrix} M \\ i & i \end{smallmatrix} \right| \alpha \left| \begin{smallmatrix} N \\ j & j \end{smallmatrix} \right| = \alpha \left| \begin{smallmatrix} M \alpha \\ i & j \end{smallmatrix} \right| N \left| \begin{smallmatrix} \\ j & i \end{smallmatrix} \right| ;$

2) $\alpha \left| \begin{smallmatrix} M \\ i & j \end{smallmatrix} \right| N \left| \begin{smallmatrix} \\ i \end{smallmatrix} \right| \alpha \left| \begin{smallmatrix} \\ j \end{smallmatrix} \right| = \alpha \left| \begin{smallmatrix} M \\ i & j \end{smallmatrix} \right| \left| \begin{smallmatrix} \\ i \end{smallmatrix} \right| N \alpha \left| \begin{smallmatrix} \\ j \end{smallmatrix} \right| ;$

3) $\left| \begin{smallmatrix} M \alpha \\ j & i \end{smallmatrix} \right| N \left| \begin{smallmatrix} \\ i \end{smallmatrix} \right| \alpha \left| \begin{smallmatrix} \\ j \end{smallmatrix} \right| = \left| \begin{smallmatrix} M \alpha \\ j & i \end{smallmatrix} \right| N \alpha \left| \begin{smallmatrix} \\ j \end{smallmatrix} \right| ;$

4) $\left| \begin{smallmatrix} \alpha \\ i & j \end{smallmatrix} \right| M \alpha \left| \begin{smallmatrix} \\ i \end{smallmatrix} \right| N \left| \begin{smallmatrix} \\ j \end{smallmatrix} \right| = \alpha \left| \begin{smallmatrix} M \\ j \end{smallmatrix} \right| \alpha \left| \begin{smallmatrix} \\ i \end{smallmatrix} \right| N \left| \begin{smallmatrix} \\ j \end{smallmatrix} \right| ;$

5) $\left| \begin{smallmatrix} \alpha \\ i & j \end{smallmatrix} \right| M \left| \begin{smallmatrix} \\ j \end{smallmatrix} \right| N \alpha \left| \begin{smallmatrix} \\ i \end{smallmatrix} \right| = \alpha \left| \begin{smallmatrix} M \\ j \end{smallmatrix} \right| \left| \begin{smallmatrix} \\ j \end{smallmatrix} \right| N \alpha \left| \begin{smallmatrix} \\ i \end{smallmatrix} \right| ;$

6) $\left| \begin{smallmatrix} M \\ j \end{smallmatrix} \right| \alpha \left| \begin{smallmatrix} \\ i \end{smallmatrix} \right| N \alpha \left| \begin{smallmatrix} \\ j \end{smallmatrix} \right| = \left| \begin{smallmatrix} M \\ j \end{smallmatrix} \right| \left| \begin{smallmatrix} \\ i \end{smallmatrix} \right| M \alpha \left| \begin{smallmatrix} \\ j \end{smallmatrix} \right| N \alpha \left| \begin{smallmatrix} \\ i \end{smallmatrix} \right| .$

VII. $\left| \begin{smallmatrix} \alpha \\ i \end{smallmatrix} \right| M \left| \begin{smallmatrix} \\ j \end{smallmatrix} \right| \alpha \left| \begin{smallmatrix} \\ j \end{smallmatrix} \right| = \alpha \left| \begin{smallmatrix} M \\ i \end{smallmatrix} \right| \left| \begin{smallmatrix} \\ i \end{smallmatrix} \right| \alpha \left| \begin{smallmatrix} \\ j \end{smallmatrix} \right| .$

VIII. $\frac{\alpha \equiv \beta}{M(\alpha) = M(\beta)}.$ *

IX. $\frac{M=N, Q(M)}{Q(N)=R}=R^*.$

* It is assumed here that $Q(N)$ is also an expression.

- X. The pair of corresponding strokes $\underline{\underline{i}}$, $\underline{\underline{j}}$, in one expression can be replaced by any other pair $\underline{\underline{j}}$, $\underline{\underline{j}}$ but so that the expression would remain an expression.
- XI. If the logical condition $\alpha \underline{\underline{i}}$ for a given shift distribution is subordinate to β , then $\alpha \underline{\underline{i}}$ can be replaced by $\alpha \& \beta \underline{\underline{i}}$.

V. A. Steklov Math. Inst.

Sept. 29, 1956

References

1. A. I. KITOV: Electronic digital machines. Moscow, 1956, p. 193.

R.I.N.S.O.

(Real Ingenious New Symbolic Optimizer)

Editor's Note: The following parody on the S.O.A.P. System is reprinted from the September 1958 issue of the Journal of Machine Accounting, Systems and Management, through the kind permission of the editor, Mr. Charles Johnson.

RINSO represents the ultimate sophisticated optimizing routine for use with the recently announced 699 Electronuclear Computing Machine. The routine allows any untrained person with an I.Q. of 40 or more to program any problem capable of definition by the human brain. Logic is taken care of by RINSO.

With RINSO, it is not necessary for the programmer to know arithmetic or any advanced mathematics. Nor must he confine himself to the use of English in his choice of symbols. The routine is capable of interpreting symbols in any of the 98 languages officially recognized by the United Nations, as well as in Uto-Aztec and Quarani.

The RINSO deck consists of three cards, one of which may be thrown away if the computer is equipped with the floating square root device. The only restriction involving the program is that it be written on a sheet of white paper measuring not more than 4' x 6'.

To prepare the machine, first drop three RINSO cards into the slot marked "THINK" on the console and place the program (s) sheet on the moving conveyor belt. Set the alpha-numeric console switches to "ANALYZE" and push the button marked "GO".

The output of RINSO consists of a printed form from the 499 Accounting Machine Listing 1) the program steps in Basic English, 2) an analysis of the program in the light of present-day computing techniques and 3) a statement of the kind and quantity of raw data necessary to make the 699 System economically feasible.

Copies of the RINSO deck may be obtained by writing to: Programmer Number 4096, Ivory Tower, Bellevue Hospital, New York, N. Y.

STANDARDS

The following is a continuation of the Standard Department's publication of the "Glossary of Computer Engineering and Programming Terminology" from the Aberdeen Proving Ground, *BRL Report No. 1010*.

The department earnestly solicits all comments concerning the proper use of terms, definitions, ambiguities and unusual meanings and applications.

PARAMETER

in a subroutine, a quantity which may be given different values when the subroutine is used in different main routines or in different parts of one main routine, but which usually remains unchanged throughout any one such use; in a generator, a quantity used to specify input-output devices, to designate subroutines to be included, or otherwise to describe the desired routine to be generated.

PARAMETER, PRESET

a parameter incorporated into a subroutine during input.

PARAMETER, PROGRAM

a parameter incorporated into a subroutine during computation. A program parameter frequently comprises a word stored relative to either the subroutine or the entry point and dealt with by the subroutine during each reference. It may be altered by the routine and/or may vary from one point of entry to another.

PATCH

section of coding inserted into a routine to correct a mistake or alter the routine; explicitly transferring control from a routine to a section of coding and back again.

PENTODE

a five-electrode vacuum tube containing a cathode, control grid, suppressor grid, screen grid, and plate.

PERFORATION, RATE of

number of characters, rows or words punched in a paper tape by a device per unit of time.

PHOSPHORESCENCE

the property of emitting light for some time after excitation.

PIEZOELECTRIC

the effect of producing a voltage by placing a stress, either by compression, by expansion, or by twisting, on a crystal; and, conversely, the effect of producing a stress in a crystal by applying a voltage to it.

PLOTTING-BOARD

a unit capable of graphically presenting information, usually as curves of one or more variables; analogue curve or point tracer.

PLUG-BOARD

a removable panel containing an ordered array of terminals which may be interconnected by short electrical leads according to a prescribed pattern and hence designating a specific program. The entire panel, pre-wired, may be inserted for different programs.

POINT

the dot that marks the separation between the integral and fractional parts of a quantity; i.e., between the coefficients of the zero and the minus one powers of the number base. It is usually called, for a number system using base two, a *binary point*; for base ten, a *decimal point*, etc; base point; radix.

POST-MORTEM

a routine which, either automatically or on demand, prints information concerning the contents of the registers and storage locations at the time the routine stopped, in order to assist in the location of a mistake in coding.

POTENTIOMETER

a variable voltage divider, a resistor which has a variable contact arm so that any portion of the potential applied between its ends may be selected.

PRECISION

the degree of exactness with which a quantity is stated; a relative term often based on the number of significant digits in a measurement. See also Accuracy.

PRECISION, DOUBLE

retention of twice as many digits of a quantity as the computer normally handles, e.g. a computer whose basic word consists of 10 decimal digits is called upon to handle 20 decimal digit quantities by keeping track of the 10-place fragments.

PRE-STORE

to set an initial value for the address of an operand or a cycle index; to restore; to store a quantity in an available or convenient location before it is required in a routine.

PROGRAM

a plan for the solution of a problem. A complete program includes plans for the transcription of data, coding for the computer and plans for the absorption of the results into the system. The list of coded instructions is called a *routine*; to plan a computation or process from the asking of a question to the delivery of the results, including the integration of the operation into an existing system. This programming consists of planning and coding, including numerical analysis, systems analysis, specification of printing formats, and any other functions necessary to the integration of a computer in a system.

PROGRAM SENSITIVE MALFUNCTION

a malfunction which occurs only when some unusual combination of program steps occur.

PROGRAMMER

a person who prepares instruction sequences without necessarily converting them into the detailed codes.

PROGRAMMING AUTOMATIC

any technique in which the computer is used to help plan as well as to help code a problem; e.g. compiling routines, interpretive routines.

PROGRAMMING, OPTIMUM

improper terminology for minimal latency coding, i.e., for producing a minimal latency routine.

PROGRAMMING, RANDOM ACCESS

programming without regard for the time required for access to the storage positions called for in the program; contrast with minimum access programming.

PSEUDO-CODE

an arbitrary code, independent of the hardware of a computer, which must be translated into computer code.

PSEUDO-RANDOM

having the property of satisfying one or more of the standard criteria for statistical randomness but being produced by a definite calculation process.

PULSE

a change in the intensity or level of some medium, usually over a relatively short period of time, e.g. a shift in electric potential of a point for a short period of time compared to the time period, i.e. if the voltage level of a point shifts from -10 to +20 volts with respect to ground for a period of 2 microseconds, one says that the point received a 30 volt 2 microsecond pulse.

PULSE-CODE

sets of pulses to which particular meanings have been assigned; the binary representations of characters.

PUNCH, CALCULATING, ELECTRONIC

a card handling machine which reads a punched card, performs a number of sequential operations and punches the result on a card.

PUNCH, CARD

a device which perforates or places holes in cards in specific locations designated by a program.

PUNCH-POSITION

the location of the row in a columnated card, e.g. in an 80-column card the rows or "punch position" may be 0 to 9 or "X" and "Y" corresponding to position 11 and 12.

PUNCH, SUMMARY

a card handling machine which may be electrically connected to another machine, e.g. tabulator and which will punch out on a card the information produced, calculated or summarized by the other machine.

PUNCHING, RATE OF

number of cards, characters, blocks, fields or words of information placed in the form of holes distribution on cards, or tape per unit of time.

QUANTITY

a positive or negative real number in the mathematical sense. The term quantity is preferred to the term number in referring to numerical data; the term number is used in the sense of natural number and reserved for "the number of digits", the "number of operations", etc.

QUANTITY, DOUBLE-PRECISION

a quantity having twice as many digits as are normally carried in a specific computer.

RANDOM-ACCESS

access to storage under conditions in which the next position from which information is to be obtained is in no way dependent on the previous one.

RANGE

all the values which a function may have.

RATIO, OPERATING

the ratio obtained by dividing the number of hours of correct machine operation by the total hours of scheduled operation, e.g. on a 168 hour week scheduled operation, if 12 hours of preventive maintenance is required and 4.8 hours of unscheduled down time occurs, then the operating ratio is $(168 - 16.8)/168$, which is equivalent to a 90 per cent operating ratio.

READ

to copy, usually from one form of storage to another, particularly from external or secondary storage to internal storage; to sense the meaning of arrangements of hardware; to sense the presence of information on a recording medium.

READ-AROUND-RATIO

in electrostatic storage tubes, the number of times a specific spot (digit or location) may be consulted before "spill over" will cause a loss of information stored in surrounding spots, immediately prior to which the surrounding information must be restored; read-around number.

READER, CARD

a mechanism that permits the sensing of information punched on cards by means of wire brushes or metal feelers.

READER, TAPE, MAGNETIC

a device capable of restoring to a train or sequence of electrical pulses, information recorded on a magnetic tape in the form of a series of magnetized spots, usually for the purpose of transferring the information to some other storage medium.

READER, TAPE, PAPER

a device capable of restoring to a train or sequence of electrical pulses, information punched on a paper tape in the form of a series of holes, usually for the purpose of transferring the information to some other storage medium.

READING, RATE OF

number of characters, words, fields, blocks or cards sensed by an input sensing device per unit of time.

REAL-TIME

the performance of a computation during the actual time that the related physical process transpires in order that results of the computations are useful in guiding the physical process.

RECORD

a listing of information, usually in printed or printable form; one output of a compiler consisting of a list of the operations and their positions in the final specific routine and containing information describing the segmentation and storage allocation of the routine; to copy or set down information in reusable form for future reference; to make a transcription of data by a systematic alteration of the condition, property or configuration of a physical medium, e.g., placing information on magnetic tape or a drum by means of magnetized spots.

REGENERATION

the process of returning a part of the output signal of an amplifier to its input circuit in such a manner that it reinforces the grid excitation and thereby increases the total amplification; periodic restoration of stored information.

REGISTER

the hardware for storing one or more computer words. Registers are usually zero-access storage devices.

REGISTER, CIRCULATING or MEMORY

a register (or memory) consisting of a means for delaying information and a means for regenerating and reinserting the information into the delaying means.

REGISTER, CONTROL

the accumulator, register or storage unit which stores the current instruction governing a computer operation; an instruction register.

REGISTER, PROGRAM

a register in the control unit which stores the current instruction of the program and controls computer operation during the execution of the instruction; control register; program counter.

REGULATION, VOLTAGE

a measure of the degree to which power source maintains its output-voltage stability under varying load conditions.

REPETITION, RATE of PULSE

the number of electric pulses per unit of time experienced by a point in a computer, usually the maximum, normal, or standard rate of pulses.

REPRESENTATIVE-CIRCULATING-TIME

a method of evaluating the speed performance of a computer. One method is to use one-tenth of the time required to perform nine complete additions and one complete multiplication. A complete addition or a complete multiplication time includes the time required to procure two operands from high speed storage, perform the operation, and store the result and the time required to select and execute the required number of instructions to do this.

RERUN

to repeat all or part of a program on a computer.

RERUN-POINT

that stage of a computer run at which all information pertinent to the running of the routine is available either to the routine itself or to a rerun routine in order that a run may be reconstituted.

RESET

to return a device to zero or to an initial or arbitrarily selected condition.

RESOLVER

a device which separates or breaks up a quantity, particularly a vector, into constituent parts or elements, e.g. to form the three mutually perpendicular components of a space vector.

RESPONSE, FREQUENCY

a measure of the ability of a device to take into account, follow or act upon a rapidly varying condition, e.g. as applied to amplifiers, the frequency at which the gain has fallen to the one-half power point or to 0.707 of the voltage gain factor; as applied to a mechanical controller, the maximum rate at which changes in condition can be followed and acted upon.

RESTORE

to return a cycle index, a variable address, or other computer word to its initial or preselected value; periodic regeneration of charge, especially in volatile, condenser-action storage systems.

RETURN

to go back to a specific, planned point in a program, usually when an error is detected, for the purpose of rerunning the program. Rerun points are usually three to five minutes apart to avoid long periods of lost computer time. Information pertinent to a rerun is available in standby registers from point to point.

REWIND

to return a film or magnetic tape to its beginning.

ROLLBACK

equivalent to rerun when referring to tape-sequenced computers; to recapture tape-inscribed data.

ROLL-OUT

to read a register or counter by adding ones to the respective digits simultaneously obtaining a signal as each column returns to zero, until all columns have returned to zero, usually requiring n additions, where n is the number base.

ROUND-OFF

to change a more precise quantity to a less precise one, according to some rule.

ROUTINE

a set of coded instructions arranged in proper sequence to direct the computer to perform a desired operation or series of operations.

ROUTINE, COMPILING

an executive routine which, before the desired computation is started, translates a program expressed in pseudo-code into machine code (or into another pseudo-code for further

translation by an interpreter). In accomplishing the translation, the compiler is required to decode, convert, select, generate, allocate, adapt, orient, incorporate, or record.

ROUTINE, DIAGNOSTIC

a specific routine designed to locate either a malfunction in the computer or a mistake in coding.

ROUTINE, EXECUTIVE

a set of coded instructions designed to process and control other sets of coded instructions; a set of coded instructions used in realizing "automatic coding"; a master set of coded instructions.

ROUTINE, FLOATING-POINT

a set of coded instructions arranged in proper sequence to direct the computer to perform a specific set of operations which will permit floating-point operation, e.g. enable the use of a fixed-point machine to handle information on a floating-point basis from an external point of view. Floating-point routines are usually used in computers which do not have built in floating-point circuitry, in which case floating-point operation must be programmed.

ROUTINE, GENERAL

a routine expressed in computer coding designed to solve a class of problems, specializing to a specific problem when appropriate parametric values are supplied.

ROUTINE, INTERPRETIVE

an executive routine which, as the computation progresses, translates a stored program expressed in some machine-like pseudo-code into machine code and performs the indicated operations, by means of subroutines as they are translated. An interpretive routine is essentially a closed subroutine which operates successively on an indefinitely-long sequence of program parameters (the pseudo-instructions and operands). It may usually be entered as a closed subroutine and exited by a pseudo-code exit instruction.

ROUTINE, MINIMAL LATENCY

especially in reference to serial storage systems, a routine so coded, by judicious arrangement of data and instructions in storage, that the actual latency is appreciably less than the expected random-access latency.

ROUTINE, RERUN

a routine designed to be used in the wake of a computer malfunction or a coding or operating mistake to reconstitute a routine from the last previous rerun point; roll back routine.

ROUTINE, SEQUENCE CHECKING

a routine which checks every instruction executed, printing certain data, e.g., to print out the coded instruction with addresses, and the contents of each of several registers, or it may be designed to print out only selected data, such as transfer instructions and the quantity actually transferred.

ROUTINE, SERVICE

a routine designed to assist in the actual operation of the computer. Tape comparison, block location, certain post mortems, and correction routines fall in this class.

ROUTINE, SPECIFIC

a routine expressed in computer coding designed to solve a particular mathematical, logical, or data-handling problem in which each address refers to explicitly stated registers and locations.

ROUTINE, TEST

a routine designed to show whether a computer is functioning properly or not.

RUN

one performance of a program on a computer; performance of one routine, or several routines automatically linked so that they form an operating unit, during which manual manipulations are not required of the computer operator.

SCALE

to alter the units in which all variables are expressed so as to bring all magnitudes within the capacity of the computer or routine at hand.

SCANNER

an instrument which automatically samples or interrogates the state of various processes, conditions, or physical states and initiates action in accordance with the information obtained.

SEGMENT

to divide a routine in parts each consisting of an integral number of subroutines, each part capable of being completely stored in the internal storage and containing the necessary instructions to jump to other segments; in a routine too long to fit into internal storage, a part short enough to be stored entirely in the internal storage and containing the coding necessary to call in and jump automatically to other segments. Routines which exceed internal storage capacity may be automatically divided into segments by a compiler.

SELECT

to take the alternative A if the report on a condition is of one state, and alternative B if the report on the condition is of another state; to choose a needed subroutine from a file of subroutines.

SELECTOR

a device which interrogates a condition and initiates a particular operation according to the interrogation report.

SENSE

to examine, particularly relative to a criterion; to determine the present arrangement of some element of hardware, especially a manually-set switch; to read holes punched in paper.

SENTINEL

a symbol marking the beginning or the end of some element of information such as a field, item, block, tape, etc.; a tag.

SEQUENCE, PSEUDO-RANDOM

an order of numbers produced by a definite recursive rule but satisfying one or more of the standard tests for randomness.

SEQUENCER

a machine which puts items of information into a particular order, e.g., it will determine whether A is greater than, equal to, or less than B, and sort or order accordingly.

SERIAL

handle one after the other in a single facility, such as transfer or store in a digit by digit time sequence.

SERVOMECHANISM

a closed loop system in which the error or deviation from a desired or pre-set norm is reduced to zero, and one in which mechanical position is usually the controlled variable, e.g., a synchronized drum storage system requires a servomechanism to insure synchronism between a crystal controlled electronic oscillator and a rotating cylinder; an AA fire control gun-positioning system requires a servo to insure that deviations are corrected.

SHIFT

to move the characters of a unit of information column-wise right or left. For a number, this is equivalent to multiplying or dividing by a power of the base of notation.

SHIFT, ARITHMETIC

to multiply or divide a quantity by a power of the number base, e.g. binary 1011 represents decimal 11, therefore two arithmetic shifts to the left is binary 101100, which represents decimal 44.

SHIFT, CYCLIC

a shift in which the digits dropped off at one end of a word are returned at the other in a circular fashion; logical, non-arithmetic or circular shift.

SIGNIFICANCE

the arbitrary rank, priority, or order of relative magnitude assigned to a given position or column in a number; the significant digits of a number are a set of digits, usually from consecutive columns beginning with the most significant digit different from zero and ending with the least significant digit whose value is known are assumed relevant, e.g., 2300.0 has five significant digits, whereas 2300 probably has two significant digits.

SIMULATION

the representation of physical systems and phenomena by computers, models or other equipment.

SKIP

an instruction to proceed to the next instruction; a "blank" instruction.

SOLVER, EQUATION

a calculating device, usually analog, which arrives at the solution to systems of linear simultaneous non-differential equations or determine the roots of polynomials or both.

SORT

to arrange items of information according to rules dependent upon a key or field contained in the items.

STACKER, CARD

a mechanism that accumulates cards in a bin after they have passed through a machine operation; a hopper.

STANDARDIZE

to adjust the exponent and mantissa of a floating-point result so that the mantissa lies in the prescribed normal range; normalize; see Floating-point Representation.

STORAGE

preferred to memory, any device into which units of information can be copied, which will hold this information, and from which the information can be obtained at a later time; devices, such as plug-boards, which hold information in the form of arrangements of physical elements, hardware, or equipment; the erasable storage in any given computer.

STORAGE, BUFFER

a synchronizing element between two different forms of storage, usually between internal and external; an input device in which information is assembled from external or secondary storage and stored ready for transfer to internal storage; an output device into which information is copied from internal storage and held for transfer to secondary or external storage. Computation continues while transfers between buffer storage and secondary or internal storage or vice versa take place.

STORAGE, CIRCULATING

a device using a delay line, or unit which stores information in a train or pattern of pulses, where the pattern of pulses issuing at the final end are sensed, amplified, reshaped and re-inserted in the delay line at the beginning end.

STORAGE, DYNAMIC

storage such that information at a certain position is moving in time and so is not always available instantly; e.g., acoustic delay line, magnetic drum; circulating or re-circulating of information in a medium.

STORAGE, ELECTROSTATIC

a device possessing the capability of storing changeable information in the form of charged or uncharged areas on the screen of a cathode ray tube.

STORAGE, ERASABLE

media which may hold information that can be changed; i.e., the media can be re-used; e.g., magnetic tape, drum, or core.

STORAGE, EXTERNAL

storage facilities divorced from the computer itself but holding information in the form prescribed for the computer; e.g., magnetic tapes, magnetic wire, punched cards, etc.

STORAGE, INTERNAL

storage facilities forming an integral physical part of the computer and directly controlled by the computer; the total storage automatically accessible to the computer.

STORAGE, MAGNETIC

any storage system which utilizes the magnetic properties of materials to store information.

STORAGE, MERCURY

columns of a liquid mercury medium used as a storage element by the delaying action or time of travel of sonic pulses which are circulated by having electrical amplifier, shaper, and timer circuits complete the loop.

STORAGE, NON-ERASABLE

media used for containing information which cannot be erased and reused, such as punched paper tapes, and punched cards.

STORAGE, NON-VOLATILE

storage media which retain information in the absence of power and which may be made available upon restoration of power; e.g., magnetic tapes, drums, or cores.

STORAGE, PARALLEL

storage in which all bits, or characters, or (especially) words are essentially equally available in space, without time being one of the coordinates. Parallel storage contrasts with serial storage. When words are in parallel, the storage is said to be *parallel by words*, when characters within words (or binary digits within words or characters) are dealt with simultaneously, not one after the other, the storage is *parallel by characters* (or *parallel by bit* respectively).

STORAGE, SECONDARY

storage facilities not an integral part of the computer but directly connected to and controlled by the computer; e.g., magnetic drum, magnetic tapes, etc.

STORAGE, SERIAL

storage in which time is one of the coordinates used to locate any given bit, character, or (especially) word. Storage in which words, within given groups of several words, appear one after the other in time sequence, and in which access time therefore includes a variable latency or waiting time of zero to many word-times, is said to be *serial by word*. Storage in which the individual bits comprising a word appear in time sequence is *serial by bit*. Storage for coded-decimal or other non-binary numbers in which the characters appear in time sequence is *serial by character*, e.g., magnetic drums are usually serial by word but may be serial by bit, or parallel by bit, or serial by character and parallel by bit, etc.

STORAGE, STATIC

storage such that information is fixed in space and available at any time; e.g., flip-flop, electrostatic, or coincident-current magnetic-core storage.

STORAGE, TEMPORARY

internal storage locations reserved for intermediate and partial results.

STORAGE, VOLATILE

storage media such that if the applied power is cut off, the stored information is lost; e.g., acoustic delay lines, electrostatic tubes.

STORAGE, WORKING

a portion of the internal storage reserved for the data upon which operations are being performed.

STORAGE, ZERO-ACCESS

storage for which the latency (waiting time) is negligible at all times.

STORE

to transfer an element of information to a device from which the unaltered information can be obtained at a later time.

SUBROUTINE

the set of instructions necessary to direct the computer to carry out a well defined mathematical or logical operation; a subunit of a routine. A subroutine is often written in relative or symbolic coding even when the routine to which it belongs is not.

SUBROUTINE CLOSED

a subroutine not stored in its proper place in the linear operational sequence, but stored away from the routine which refers to it. Such a subroutine is entered by a jump, and provision is made to return, i.e., to jump back to the proper point in the main routine at the end of the subroutine.

SUBROUTINE, DYNAMIC

a subroutine which involves parameters, such as decimal point position or item size, from which a relatively coded subroutine is derived. The computer itself is expected to adjust or generate the subroutine according to the parametric values chosen.

SUBROUTINE, OPEN

a subroutine inserted directly into the linear operational sequence, not entered by a jump. Such a subroutine must be recopied at each point that it is needed in a routine.

SUBROUTINE, STATIC

a subroutine which involves no parameters other than the addresses of the operands.

SUBSTITUTE

to replace an element of information by some other element of information.

SWITCH, ELECTRONIC

a circuit which causes a start-and-stop action or a switching action by electronic means.

SWITCH, FUNCTION

a circuit having a fixed number of inputs and outputs designed such that the output information is a function of the input information, each expressed in a certain code or signal configuration or pattern.

SYMBOL, LOGICAL

a symbol used to represent a logical element graphically.

SYSTEM

an assembly of components united by some form of regulated interaction; an organized whole.

TABULATOR

a machine which reads information from one medium, e.g., cards, paper tape, magnetic tape, etc. and produces lists, tables, and totals on separate forms or continuous paper.

TAG

a unit of information, whose composition differs from that of other members of the set so that it can be used as a marker or label; a sentinel.

TANK

a unit of acoustic delay line storage, containing a set of channels each forming a separate recirculation path; a circuit consisting of inductance and capacitance used for the purpose of sustaining electrical oscillations.

TAPE, MAGNETIC

a tape or ribbon of any material impregnated or coated with magnetic material on which information may be placed in the form of magnetically polarized spots.

NEWS AND NOTICES

ACM CHAPTER NEWS

Delaware Valley Chapter:

The Delaware Valley Chapter is proud to announce that since its inception in June, membership has passed the 100 mark.

For the August meeting, Richard Todd of General Electric, Program Committee Chairman, invited John Waite of RCA, Camden, New Jersey to speak on "Programming Techniques As Affecting the Design of Large Scale Data Processing Systems."

Houston Chapter:

At its September 24 meeting the Houston Chapter heard Dr. William Tobocman of the Physics Department at Rice Institute and Research Associate at the Computing Center at the University of Houston, speak on "A Numerical Calculation in Nuclear Physics."

Kansas City, Missouri Chapter:

Robert J. Olson, Chairman, Kansas City ACM, reports that a group of members of the Los Angeles Chapter have been transplanted to Kansas City at the System Development Corporation Sage Site. The group has submitted bylaws, petitioned for affiliation to the National ACM, and formed a local chapter. Its first meeting is scheduled for mid-October.

Los Angeles Chapter:

A more thorough description of the September 3 meeting at which Dr. Morris Rubinoff, Chief Engineer of Computers, Philco Corporation, spoke on the topic, "Through Europe, Bit by Bit":

Dr. Rubinoff described his recent European tour on which he visited computer installations, and organizations active in the computing field in Scotland; England (at Manchester University—the Ferranti Mercury computer; at the Ferranti Company—the Pegasus and Mercury computers; and at the English Electric Company—the DEUCE); Italy (the Olivetti); Israel; Switzerland; Germany; Denmark; Sweden; France (Bull Manufacturing Company—the Gamma 60); Belgium; Finland; and Holland. Dr. Rubinoff's over-all opinion was that Europe is now at the vacuum stage of computer development; in general, transistorization has just begun to appear. Design is basically serial synchronous, and diodes and junctional alloy transistors are used primarily. Inexpensive nickel delay lines are being used extensively to incorporate numerous logical tricks at a low cost. Magnetic cores are also being used in ingenious ways. The input-output equipment is generally slow, usually by paper tape at 33 characters per inch. Magnetic tape speeds, however, are 100 inches per second. Cabinet design is poor from the standpoint of United States taste. The most severe limitation to European computer development is the nationalistic attitude toward merchandising between countries. The resultant limited market keeps production at a low scale.

Dr. Rubinoff concluded that Europe is 1-2 years behind the U. S. from the standpoint of technology, but not from the standpoint of ingenuity. He also feels that European machines will influx to the United States soon.

St. Louis Chapter:

The tentative programs for St. Louis Chapter meetings are as follows: October—"Market Research;" November—"Digital Differential Analyzer;" January—"Network Analysis;" February—"Linear Programming;" March—"Process Control;" and April—"SAGE."

San Diego Chapter:

At the August 7 meeting of the San Diego Chapter, Dr. S. Chandrasekhar, Professor of Theoretical Astrophysics at the University of Chicago, spoke on partial differential equations. He bridged the gap between technical and non-technical by illustrating his mathematical work with descriptions of physical systems.

At a meeting on September 18, Mr. Henry Taylor of the Stromberg Carlson Division of General Dynamics gave a talk on the many uses of charactron readout systems.

Washington, D. C. Chapter:

The Washington, D. C. Chapter held a dinner meeting on August 13 at the Broadmoor Hotel where Dr. Joseph Wegstein of the National Bureau of Standards spoke to over 70 members on "The Future of Automatic Programming Systems." Dr. Wegstein reviewed such topics as BO, SAP, USE and SOAP.

At the September 17 meeting Mr. John Backus, Manager of Programming Research, IBM, reviewed the proposed ACM-GAMM international programming language.

The chapter is establishing an education committee, which will develop and organize a computer lecture series and other appropriate computer courses for local high schools.

Any ACM member interested in joining the Washington Chapter should contact Mr. Lowell McClung at the Johns Hopkins University Applied Physics Laboratory.

COOPERATIVE PROGRAMMING GROUPS

SHARE

The eleventh meeting of SHARE, held in San Francisco on September 10-12, was attended by 300 delegates representing over 100 installations. Current membership is 112; of these, 93 hold "IBM 704" memberships and 55 hold "IBM 709" memberships; 36 installations fall into both categories.

New officers elected at the meeting include: President, B. Ferber of Convair, San Diego, California; Vice President, H. Bright of Westinghouse Bettis, Pittsburgh, Pennsylvania; and Secretary, J. Koory of System Development Corporation, Los Angeles, California. Members of the Executive Board are W. Ramshaw of United Aircraft, F. Verzuh of Massachusetts Institute of Technology, E. Jacks of General Motors, and F. Wagner of North American Aviation (past President).

The most significant development of the meeting was the wholehearted backing by SHARE of the international algebraic language standardized by representatives of ACM, in the United States, and of GAMM, their counterpart in Germany and Switzerland. This standardization upon a problem-oriented algebraic language is a parallel, not an alternative, development to the investigations being conducted by the UNCOL (Universal Computer-Oriented Language) Committee. The SHARE president will appoint an ad hoc committee on algebraic language to study the proposed international language and implement its adoption as a SHARE standard.

During the meeting IBM announced tentative specifications for an optional feature, known as the "DS Trap," for the 709 computer. This feature, requested by SHARE, will permit the data synchronizer to signal the main frame, with each channel trapping to a unique location.

In spite of a strong effort to standardize, several different automatic operator programs are being used on the IBM 709's just being delivered in the field now. A sizeable subgroup is writing a common monitor system which will include automatic accounting and tape handling and will run stacked jobs of all kinds in three distinct phases.

The standard form for distributing all 709 programs has been established to be a binary card deck which contains the program in symbolic form but encoded for efficient storage. Such decks can only be produced by and read by a machine.

Although 709 and FORTRAN matters dominated the agenda, there were three interesting developments in the 704 machine language field. The 704 Data Processing Committee promises a versatile system ready for field trials by the first of the year, as does the SPADE Subcommittee on partial differential equations. Most novel is the projected version of SCAT for the 704; delivery dates for this are not firm.

Bendix G-15 Users EXCHANGE

Approximately 200 users attended the third national conference of the Bendix G-15 Users EXCHANGE organization held on September 25-26 at the Drake Hotel in Chicago. Manufacturers whose products are compatible with the G-15 exhibited their equipment at the conference (plotters, tape punches, verifiers and other tape handling equipment). Speeches were presented on various topics including: Pro-

gramming Methods; Effective Use of a Medium Sized Computer; Automatic Coding for the G-15; Statistical Applications; The Use of Two-Word Registers; Digital Recording and On-Line Use; Automatic Programming; Floating Point and Scaling; and Magnetic Tape. The Committee on Civil Engineering Applications extended the conference to September 27 to hold a regular quarterly meeting. This meeting included workshops on highway and structural applications.

NEWS ITEMS

- The IBM 7070, a completely transistorized computer in the intermediate price field, has recently been developed by International Business Machines Corporation. By using transistors, installation and environmental cost has been cut by one-third. The system is based on a modular design and can be operated from cards and/or magnetic tapes. Four files of 50 magnetic disks can be included to provide random access storage of 24-million digits. Time is saved by overlapping machine operations; through the use of two tape channels, the 7070 is able, while computing, to read or write magnetic tapes (Type 729) at the rate of up to 125,000 characters per second. Also, it can handle simultaneously three 400-card-a-minute readers and three 250-card-a-minute punches. Its new features include automatic double precision floating point operations; Automatic Priority Processing (an automatic interruption feature); "Scatter Read-Write" (permits writing records on tape from "scattered" data in core storage without assembling the data internally); Tape Compression (automatic zero elimination for tape reading and writing); and a complete complement of indexing instructions with 99 index words.
- The Philco Corporation has announced the C-1100, a transistorized airborne computer. The computer performs 64,000 additions or 16,000 square roots per second. Designed to handle all computational requirements to control a jet aircraft from take-off to landing, the drum storage of the computer can retain from 1,500 to 5,000 instructions or numbers as twenty-bit words. The computer occupies less than three cubic feet of space, weighs about 150 pounds, and uses 60 watts of direct electric current.
- Stanford Research Institute reports the development of a magnetic read head for the automatic reading of letters and numerals printed in magnetic ink; it will also be useful with magnetic drums and magnetic tape transports. The read head allows recording at 83 channels per inch. Crosstalk was a difficult design factor since each channel occupies only 0.012 inches, including the space between heads.
- Philco Corporation and the Uptime Corporation of Rawlins, Wyoming, have announced a joint program to develop and market a new high speed punched card reader known as "Speed-reader 2000." The prototype model for this new machine reads conventional 80-column punched cards, row by row, at the rate of 2000 cards per minute. Its feed and stacking hoppers can hold 4000 cards.
- IBM has announced the availability of punched card output on its 632 Electronic Typing Calculator. The 632 automatically does the arithmetic on business forms as they are filled out by a typist. The card output will enable the integration of the 632 into further machine processing. For example, invoice preparation on a 632 can now simultaneously create the card input for a sales analysis, an inventory, or a chart of accounts receivable.
- Amp, Inc., of Harrisburg, Pennsylvania has developed a light-weight patchcord programming system designed for reprogramming of airborne circuitry. Known as the 240 System, the device has been miniaturized to conserve space and weighs only 3½ pounds. Removable, pre-patched boards make complete circuitry reprogramming possible in a matter of seconds.
- Another patchcord programming system, an extension of multiple contact connectors beyond the point where such connectors can be used manually, is the product of Virginia Electronics Company, Inc., of Washington, D. C. The flexibility of the system is a result of the modular arrangement of specially designed contact strips of 22 contacts and the fact that the programming may be accomplished by the use of single patchcords or permanent wiring. In the case of permanent programming it is perfectly feasible to wire in such resistors, capacitors, etc., as may be required for certain specific uses without increasing the size of the programming board in any way. (Courtesy *Datamation*)
- National Vulcanized Fibre Company of Wilmington, Delaware has developed a thin vulcanized fibre tape, .005-inch thick, designed for use on punched tape controlled automatic programming equipment. According to the manufacturer this cellulose plastic tape has a tensile strength of better than 600

psi, high density, low porosity, excellent abrasion resistance, is easily punched, will not stretch out of shape during use, and produces a minimum of wear on the perforating and feeding equipment associated with tape control applications.

- Alwac Computer Division of El-Tronics, Inc. has compiled the statistics on ALWAC III-E uptime into regional reliability figures (a function of total computer time in production operation versus total required computer operation time): Eastern Region, 96.1 per cent; Western Region, 97.1 per cent; and national average 96.6 per cent.

- At the Airpower Panorama in Dallas, an IBM 305 RAMAC system was used to store thumbnail biographical sketches of Air Force general officers. Upon demand the system would output historical information on the Air Force or biographical information on any one of the 300 general officers of the Air Force.

- The National Bureau of Standards, in conjunction with the National Science Foundation, is planning to hold its second "Training Program in Numerical Analysis for Senior University Staff" during the spring term of 1959. Regular university staff members will be given training in numerical analysis to enable them to direct the operation of a university computing center and other activities in this field.

- It has been announced that an elaborate data processing center will be presented to Brown University as a gift. The Center will be established in memory of the late Thomas J. Watson, Sr., former president and chairman of the board of International Business Machines Corporation.

- The General Electric Company, Aircraft Gas Turbine Division has announced the development of an automatic information retrieval system, mechanized on the IBM 704 computer. All technical documents in the AGT library are identified in terms of descriptive key words. Each document may have a dozen or more words to describe it, and all documents pertaining to the same subject will be listed by number with these words. In addition, a description abstract is prepared for each document in the system. The information is recorded on magnetic tapes. At present there are more than 30,000 abstracts and 7,000 key words describing the documents. Using the IBM 704 the entire list of $\frac{1}{4}$ -million file numbers can be searched in less than three minutes. In less than 15 minutes, the time depending on the number of documents found during the search, the system will deliver printed abstracts of those documents. The system has a capacity, in its present form, for 1,000,000 abstracts and 56,000,000 file numbers.

- IBM has announced that it will officially announce on January 1, 1959 the 709-TX computer. The first machine will be available in early 1960. The 709-TX will be completely solid state and will have a computing speed four to six times faster than the 709. It will utilize a two-microsecond cycle core storage. Except for data transfers to the drum and to the cathode ray tube, 709-TX programs will be directly compatible with the 709 and will be compatible with the 704 with the aid of a "package."

- An IBM 650 RAMAC System has been installed at Indianapolis, Indiana, in conjunction with the C.A.A. Technical Development Center. The computer, referred to as the first electronic computer placed in operational service by the C.A.A. in modernizing air traffic control, will be used to record and process aircraft flight plan data. The system will maintain a complete record of flight plans, flight progress strips, airways and fix tables, and other traffic control data, for immediate availability to the controller. An IBM 407 accounting machine is used to print flight progress strips at a maximum rate of 3,000 strips per hour. Two IBM 838 inquiry stations are used in the system to input special data relating to aircraft movements and situations. The 650 RAMAC System will also perform processing to determine conflicts in aircraft movements.

- The Alwac Users Association Newsletter reports that two demonstration routines of historical interest have been devised. One, by G. A. Bachelor, calculates directly in Roman numerals and also carries out Arabic-Roman and Roman-Arabic conversion. The other, by H. E. Goheen, converts a fraction into a sum of "unit fractions," that is, fractions with a unit numerator. This is a form of the method used by ancient Egyptians to handle rational numbers.

Also, Gustav Lochs, visiting mathematics professor from University of Innsbruck, Austria, during 1958-1959, coded, for ALWAC, calculations concerned with continued fraction representations of rational numbers. A paper on this program will appear in a European journal.

- Beckman Systems of Anaheim, California is providing a complex data processing system for use at the NACA Langley Aeronautical Laboratory at Langley Field, Virginia. A Model 210 data logger will be used to sample wind tunnel information at the rate of 3,000 signals per second. The information from transducers within the tunnel being served will be fed to the system and recorded as temperatures, pressures, flows, shaft positions and other variables. The system is being built entirely around solid-state components. (Courtesy *Datamation*)
- The first Burroughs 205 computing system to be shipped overseas will be installed at the South African National Life Assurance Company (Sanlam). This is also the first application of U. S.-style automation to insurance policy handling in South Africa.
- An IBM 705 was installed at the Confederation Life Association in Toronto, Canada. It is estimated that this 705, the first in the Canadian life insurance industry, will have paid for itself in little more than five years.
- The Office of Ordnance Research, U. S. Army, is sponsoring work on non-linear integral equations. A. T. Lonseth, G. A. Bachelor, and J. E. McFarland will be employed on the project, and an ALWAC III-E will be used for the numerical solutions. Previous work on integral equations was sponsored by OOR (1952-1956) and Wright Air Development Center (1955-1956).
- The July/August issue of *Datamation* Magazine reports that Epseco, Inc. has delivered and installed an automatic, multi-channel data acquisition and computer linkage system at the Engineering Research Laboratories, Republic Aviation Corporation, Farmingdale, Long Island, New York. The system is being used initially to control data from air frame structural tests; wind tunnel instrumentation applications will follow. The present system processes structural analysis data from 200 low-level strain gauge sources; sequences, amplifies, samples and converts the data into digital form at rates up to 4000 converters per second; and prepares magnetic tape for direct entry into a 704.
- Recent appointments at General Electric's Missile and Space Vehicle Department, Philadelphia, Pennsylvania include: Philip Ravitch, formerly Senior Methods Analyst, Remington Rand Univac; Arthur Root, formerly with General Electric in Utica, New York; and Jordan Rabin, formerly with the ElectroData Division of Burroughs Corporation.
- Sol Zechtor has recently been promoted to Manager of the Transistorized Devices Laboratory of Philco Corporation's Government and Industrial Division.
- McLain B. Smith, formerly Assistant General Manager of the Data Processing Division, has recently been named a Vice President of International Business Machines Corporation.
- Arnold B. Schacknow, formerly of Republic Aviation Corporation, has accepted a position as Head, Computational Laboratory, at the Arma Division of American Bosch Arma Corporation, Garden City, New York.
- Walter G. Edwards, formerly Chief Engineer for The National Cash Register Company, Electronics Division, has joined Marc Shiowitz and Associates, Inc., Gardena, California, consultants and engineers in the electronic computer field.
- The Thompson-Ramo-Wooldridge Products Company of Los Angeles, California, which specializes in industrial control and data reduction systems, recently announced the following appointments: Thomas M. Stout as manager of the Process Applications Department, which plans computer control systems for selected processes in the petroleum refining and chemical industries; James A. Trapp as manager of the Data Processing and Controls Department, which studies new applications for computer control systems; William S. Aiken as manager of the Project Engineering Department, which handles the installation and checkout of computer control and data logging systems; and Henry L. Bechard as Customer Relations Manager.
- Recent additions to the technical staff of the Computation and Data Reduction Center at Space Technology Laboratories include J. Riley, who is assigned to the Numerical Analysis Section and L.

Turner, who is with the Applied Mathematics Section. In addition, Dr. A. V. Balakrishnan of U.C.L.A. has been retained as a consultant for the organization.

• Dorothy Arnold of Computer Controls Corporation in Los Angeles, California was chosen Chairlady of the Government Committee for the Los Angeles ACM Council.

• George Masurat has recently been promoted to General Superintendent of Production for Philco Corporation's Government and Industrial Division.

• Dr. Fletcher W. Donaldson, formerly of General Electric Company's Missile and Space Vehicle Department, has joined The Thompson-Ramo-Wooldridge Corporation for assignment to Ft. Huachuca, Arizona.

• William Gunning, formerly of Beckman Instruments, is now with Epsco, Inc. He will manage the newly-formed western office of Epsco in Los Angeles.

• "Mathematics Serving Man" is the theme of a new corporate advertising program which was recently launched by International Business Machines Corporation. Designed to increase public awareness of the contribution to man's progress made by mathematics and to encourage mathematical careers among young people, the advertisements tell the story of great milestones in man's mathematical learning, from his earliest efforts at counting through such advanced concepts as Von Neumann's theory of games. The series will be featured in such magazines as *Newsweek*, *Time*, *U. S. News and World Report*, *Science World*, and *Senior Scholastic*.

• Six analog-digital converters are detailed in an eight-page booklet published by Kefratt Company, Inc., Engineering and Sales Division, 1500 Main Avenue, Clifton, New Jersey. Included in the brochure are code patterns for each converter model which visually depict the actual arrangement of bits on each drum and a tabulation giving values for operating and other characteristics.

• A brochure describing the model MC-400 desk-size analog computer is now available from Mid-Century Instrumatic Corporation, 611 Broadway, New York 12, New York. The booklet describes in detail the operational amplifiers and other standard and optional equipment including removable patch-boards.

• Consolidated Electrodynamics Corporation at 300 N. Sierra Madre Villa, Pasadena, California, publishes a two-page bulletin, No. 1608, on the type 5-680 digital magnetic-tape recorder/reproducer. The unit is all-transistorized, stops and starts in less than three milliseconds, has all-metal-surface magnetic heads, continuous duty servo motors, and handles tape widths from $\frac{1}{2}$ inch to one inch.

• At the annual meeting of the Northwest Computing Association, held at the Benjamin Franklin Hotel in Seattle, Washington, Colonel Wilford D. Gower, Sixth U. S. Army and Comptroller at Fort Lewis, described how automation of data processing will save vast sums of money in the operation of army installations throughout the country. Colonel Gower compared military inventory, cost accounting, fiscal, and works maintenance operations to similar functions in business and industry.

At the regular monthly meeting of this association in September, installation of the following officers took place: President, Jackson W. Granholm, Senior Group Engineer of Boeing's Flight Test Operations (and editor and publisher of *Computing News*); Vice President, Hilton U. Brown, III, Associate Engineer at Puget Sound Power and Light; Secretary, Valdo Volta of Electronic Data Processing Research at Northwestern Mutual Insurance Company; and Treasurer, Donald E. Neilan of Boeing Aircraft. New council members include Robert D. Aeder of IBM; Dr. David B. Dekker, Professor of Mathematics and Director of the Computing Laboratory at the University of Washington; Harry Ostling of Sperry Rand Univac; and John F. Stockman of Boeing Aircraft Company.

Inquiries on future meetings of the Northwest Computing Association or membership applications should be addressed to Box 836, Seahurst, Washington.

• The International Association for Analog Computing held an international symposium in Strasbourg, France in September on the problems of analog computation. The symposium was divided into three sections: mathematical and physical problems in analog computers, diverse applications, and simulators and relations between analog and digital computers.

- The Mid-Continent Computer Club (MC²) held a dinner meeting on October 3 in Chicago. Preston C. Hammer, Professor of Mathematics and Director of the Numerical Analysis Laboratory at the University of Wisconsin, spoke on "Numerical Analysis, Information and Computing." A discussion period followed the speech.
- At the September 18 meeting of the Southern California Meter Association Mr. Jack K. Walker, Department Manager, Systems Division, Consolidated Electrodynamics Corporation spoke on the topic, "Computer Controlled Pilot Plant." Mr. Walker explained that a small catalytic pilot plant, called the Micro-plant, has been designed for use in process analysis and development studies. The Micro-plant is equipped with a graphic panel, continuous analyzers, electronic controls, scanning, logging, digital computer, and programmer. After an engineer feeds in a catalyst and gives initial instructions, a desk-size computer automatically conducts round-the-clock tests, some lasting for weeks, constantly analyzing raw materials and products. The computer also resets the plant operational program.
- The Burroughs Corporation has recently been awarded a \$17,418,352 Air Force contract for the construction of 24 coordinate data processing systems to be used in the SAGE system of continental air defense.
- The Digital Computers Association in Los Angeles, California invited Mr. J. Svigals, Special Representative, IBM Western Regional Staff, to give a detailed description of the new IBM 7070 at the September DCA meeting.
- At the annual Instrumentation Conference of the Instrument Society of America in September, the Standard Oil Company, Ohio, and The Thompson-Ramo-Wooldridge Products Company, Los Angeles, California announced a cooperative development study to explore new automation frontiers for the control of Standard Oil's refinery units. Based on the "systems engineering" approach to process optimization, the study is expected to develop new digital computer control techniques and equipment to meet control requirements.
- A German subsidiary, Consolidated Electrodynamics Corporation, GmbH, will serve as a central sales and service facility for the parent California firm in Western Europe and the United Kingdom. The wholly owned subsidiary will provide improved and direct factory service to users of CEC's data processing instrumentation and analytical and control equipment. A. W. Brandmaier is manager of the German company.
- Sylvania Electronic Systems, a division of Sylvania Electric Products, Inc., recently opened a 102,000 square foot facility in Needham, Massachusetts to house a data processing laboratory. Work will include development of Ballistic Missile Early Warning Systems for the Air Force and the Mobile Digital Computer System for the Army.
- The 1958 Computer Applications Symposium was held on October 29-30 at the Morrison Hotel in Chicago, Illinois. This symposium, sponsored by the Armour Research Foundation of Illinois Institute of Technology, was divided into two sessions—Business and Management Applications, and Engineering and Scientific Applications. Speeches were delivered on the following topics: Operations Research and the Automation of Banking Procedures; Information Systems Modernization in the Air Materiel Command; Utilization of Computers for Information Retrieval; Problems and Prospects of Data Processing for Defense; An Integrated Data-processing System; Input-Output, Key or Bottleneck?; Scientific Uses of a Medium-Scale Computer with Extensive Accessory Features; Optimizing Designs with Computers; Computer Applications in the Numerical Control of Machine Tools; Frontiers in Computer Technology; Computer Sharing by a Group of Consulting Engineering Firms; Current Developments in Computer Programming Techniques; and The Future of Automatic Programming.
- The Friden Company will present a special Forum on Integrated Data Processing Machines in Seattle November 11-14. The tape operated machines to be displayed will include the Selectadata, Teledata, solenoid printers, add punch machines, Flexowriters, Justowriter, Computyper, and Flexowriters with tab card input and Flexowriters with tab card output, etc.

- The "Interdisciplinary Conference on Self-Organizing Systems" will be held on May 5 and 6, 1959, at the Museum of Science and Industry, Chicago, Illinois. Sponsored by the Information Systems Branch of Office of Naval Research and Armour Research Foundation of Illinois Institute of Technology, the conference will include discussions on the general theory of the learning and cognitive processes, as well as its applications to the design of automata having properties frequently referred to as adaptive. For further information contact Scott H. Cameron, Electrical Engineering, Research Department of Armour Research Foundation, 10 West 35th Street, Chicago 16, Illinois.

COMING EVENTS

- Forum on Integrated Data Processing Machines
November 11-14, 1958; Seattle, Washington
Sponsor: Friden Company
Contact: E. O. Blix, District Manager, Friden Co., 2332 Second Avenue, Seattle, Washington
- International Conference on Scientific Information
November 16-21, 1958; Mayflower Hotel, Washington, D. C.
Sponsor: National Academy of Sciences, National Research Council, National Science Foundation, American Documentation Institute
Contact: Secretariat, International Conference on Scientific Information, National Academy of Sciences, 2101 Constitution Avenue, N. W., Washington, 25, D. C.
- Federal Government Accountants Association Eighth Annual Symposium
November 17-18, 1958 (Theme: "Management & Electronic Data Processing")
Contact: M. C. Powers, 1523 L Street, N. W., Washington 5, D. C.
- American Mathematical Society Meetings
November 20-21, 1958; Pomona, California
and
November 28-29, 1958; Northwestern University, Evanston, Illinois
and
November 28-29, 1958; Durham, North Carolina
- Computer Exhibition and Business Symposium
November 28-December 4, 1958; London, England
Contact: Exhibition Organizer, 11/13 Dowgate Hill, London E.C. 4, England
- Eastern Joint Computer Conference
December 3-5, 1958; Bellevue-Stratford Hotel, Philadelphia, Pennsylvania
Contact: John Broomall, Dev. Engr., Burroughs Corporation, Research Center, Paoli, Pennsylvania (General Chairman); F. M. Verzuh, Asst. Director, Computation Center, M.I.T., Cambridge, Massachusetts (Technical Program Chairman)
- USE Meeting
December 10-12, 1958; El Paso, Texas
- American Mathematical Society Meetings
January 20-22, 1959; University of Pennsylvania, Philadelphia, Pennsylvania (65th Annual Meeting)
and
February 28, 1959; New York, New York
- Western Joint Computer Conference
March 3-5, 1959; Fairmont Hotel, San Francisco, California
Contact: M. L. Lesser, IBM Research Lab, San Jose, California
- USE Meeting
April 1-3, 1959; Chicago, Illinois

- American Mathematical Society Meetings
April, 1959; Monterey, California
April, 1959; New York, New York
- Joint Meeting of Institute of Mathematical Statistics (Central Region) and the Association for Computing Machinery
April 2-4, 1959; Case Institute of Technology, Cleveland, Ohio
Contact for IMS: Martin B. Wilk, Bell Telephone Laboratories, Murray Hill, New Jersey
Contact for ACM: Daniel Teichroew, National Cash Register, Dayton 9, Ohio
- Interdisciplinary Conference on Self-organizing Systems
May 5-6, 1959; Museum of Science and Industry, Chicago, Illinois
Sponsor: Information Systems Branch, Office of Naval Research and Armour Research Foundation of Illinois Institute of Technology
Contact: S. H. Cameron, Armour Research Foundation, 10 W. 35 Street, Chicago 16, Illinois
- 1959 Electronic Components Conference, "New Concepts for Space Age"
May 6-8, 1959; Benjamin Franklin Hotel, Chestnut Street at 9th, Philadelphia, Pennsylvania
Sponsors: AIEE, IRE, EIA, WCEMA
- First International Conference on Information Processing (ICIP)
June 15-20, 1959; Paris, France
Sponsor: UNESCO
Contact for U. S. Committee of ICIP: A. S. Householder, Chairman, U. S. Program Committee, Oakridge National Laboratories, P. O. Box X, Oakridge, Tennessee
- 1959 ACM National Conference
Summer, 1959; Massachusetts Institute of Technology, Cambridge, Mass.
Contact: F. Verzuh, M.I.T., Computation Center, Cambridge, Mass.
- American Mathematical Society Meetings
June, 1959; Far West
and
Summer, 1959; Salt Lake City, Utah
and
November, 1959; Detroit, Michigan
- Eastern Joint Computer Conference
1959; Boston, Massachusetts
- Second Interkama—International Congress and Exhibition for Measuring Techniques and Automation
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OFFICE OF NAVAL RESEARCH · MATHEMATICAL SCIENCES DIVISION

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Gordon D. Goldstein, Editor
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The purpose of this newsletter is to provide a medium for the interchange among interested persons of information concerning recent developments in various digital computer projects. Distribution is limited to government agencies, contractors, and contributors.

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Approved by
The Under Secretary of the Navy
20 August 1957

NAVEXOS P-645

COMPUTERS AND DATA PROCESSORS, NORTH AMERICA

MANIAC III - UNIVERSITY OF CHICAGO - CHICAGO, ILLINOIS

The arithmetic unit of Maniac III has two separate and distinct modes of operation. The first is the familiar floating point system with the exception that the usual normalization step at the end of each operation is omitted. Instead, the treatment of results corresponds to one of several possible significant digit arithmetics. A complete discussion is in press. The second mode is an unconventional fixed point scheme that permits wider application with greater ease. Indeed double, or multiple precision floating point arithmetic can be handled in a rather straight-forward manner with this approach.

Construction of the arithmetic unit of Maniac III is approximately one-half completed. All arithmetic registers and the adder are finished, and are under test operation with a minimum section of the control. Surface-barrier and micro-alloy transistors are used throughout. All circuits are assembled on etched circuit cards (double-sided) which are inserted into multiple contact connectors. A novel form of gating circuit is employed which relies principally on diodes for logical elements, and minimizes the need for transistors. All circuits are direct coupled, and the control is asynchronous. About 4,000 transistors and 16,000 diodes are needed for the complete arithmetic unit.

AUTOMATIC ERROR-CORRECTION - DATAMATIC - NEWTON HIGHLANDS, MASSACHUSETTS

DATAmatic Division of Minneapolis-Honeywell has developed ORTHOTRONIC CONTROL, an automatic error correction technique which almost entirely overcomes tape errors.

The DATAmatic tape is divided into 36 tracks or channels which extend longitudinally along the tape. 31 of these channels are used to store information words, of which 62 can be recorded in a unit block on tape. Of the remaining 5 channels, one is a spare, three are allocated for control purposes and one is the Monitor Channel (Orthochannel). The words are recorded in a staggered fashion on every other block with the tape moving in a forward direction. At the physical end of the tape the motion is reversed and the alternate blocks are recorded. It is in this manner that the interlace recording system of the DATAmatic 1000 omits the usual "dead" spaces required for tape acceleration and deceleration.

Each DATAmatic word is composed of a collection of 52 binary zeroes and ones numbered from 1 through 52 when read from right to left. The four bit (binary digit) positions on the extreme right of each word (positions 1 through 4) are employed as the Weight Count digit, a checking device. This 4-bit digit is automatically generated and appended to each 48 bits of information introduced or generated with the computer. It provides a verification of the accuracy of all word transfers and arithmetic and logical manipulations. It is important to note that every word, be it numeric, alphanumeric, or instruction, is treated as numeric (4-bit) for the computation of its weight count.

Associated with each of the 48 information bits in a word is a number 1, 2, 4, or 8 called the weight for the related bit position. For example, bit positions 5, 6, 7, and 8 have the weights of 1, 2, 4, and 8 respectively. The weight count of each word is determined as follows and appears in bit positions 1 through 4.

1. Calculate the decimal sum of the weights where binary ones occur in bit positions 5 through 52.
2. Divide this sum by nine and obtain a remainder digit having a value of from zero to eight.
3. If the remainder digit is zero, the weight count appears as a nine.

4. If the remainder digit has a value of from 1 to 8, the weight count digit is precisely this value.

Whenever a word is transferred from the Input Buffer to memory, the weight count is recomputed and checked against the original. If an incorrect count is detected indicating that the word is incorrect, the DATAmatic 1000 utilizes ORTHOTRONIC CONTROL to regenerate the original information. It is important to note that this procedure is initiated only when an error is evident.

To simplify the explanation of the development of the Orthochannel, only three data channels will be considered although the same reasoning will apply when using up to 31 channels. If the sum of the "1" bits in position 52 of words 1, 3, and 5 is an odd number, then Orthobit 52 of the word in the Orthochannel is a "1." However, if there is an even number of "1" bits in those information positions, bit 52 of the Orthochannel is a "0". This Orthoaddition method of construction is repeated for all information and weight count bits of the odd-numbered words. This produces the first 52 bits of the Orthochannel, and constitutes the first Orthoword. Furthermore, this process is repeated for the even-numbered words within that block to obtain the second set of 52 bits to complete the construction of the Orthochannel. It should be pointed out that all 52 Orthobits are summed simultaneously.

The procedure described above occurs in circuitry which is located between the memory and the Output Buffer section of the computer. This Output Buffer is a temporary storage location for 62 words prior to their transfer to magnetic tape. By the time all 62 of the data words that are to be written as a block of information on the tape have been assembled in the Output Buffer, the two words of the Orthochannel have been constructed and are ready for the actual recording operation. This process, therefore, requires no additional machines or programming time. When the appropriate instruction is given by the Control Unit of the system for writing on tape, 32 channels are recorded simultaneously—31 channels of information and the Orthochannel. This then completes the first phase of the operation.

When, at some subsequent time, the information on this tape is read back into the Central Processor, it is at this point that the actual corrective procedure will be initiated, if necessary. When the instruction is given via the Control Unit to read the tape, all 32 channels are read simultaneously into the Input Buffer section. The next step in the normal sequence of operation is to transmit the information from the Input Buffer to the Memory section of the machine. It is at this stage that data is verified for accuracy by applying the normal weight count check. If the information content (the first 48 bits) of a word does not agree with its weight count, it is known that this word has certain inaccuracies within the body of its information. Previously when this was determined, certain alternatives were open to the programmer. He could stop the machine or could attempt to re-read the information in the hope that upon the second reading the information would be found to be correct. With Orthotronic Control, however, an entirely different and completely constructive action is taken. If the word is found to be inconsistent with its weight count, the operation is directed to memory register 1987. The instruction stored in 1987 leads to a subroutine, devised by the programmer, which used the Orthochannel to correct the error. Before initiating the correction procedure, the subroutine may, as one of many alternatives, cause the entire block of data to be re-read from tape into the buffer. A new Orthomonitor Transfer In instruction, one which includes the transfer of the Orthotronic Monitor Channel, is then used to bring into memory the entire block. When all 64 words have been entered into memory a special Add instruction, which has been included in the repertoire of instructions, then enables the machine to regenerate the original data. If, for example, an error exists in an odd-numbered word, all other odd-numbered words in that block (including the Orthoword) are specially summed by this newly-developed instruction and the result obtained is the authentic, original and correct version of the inaccurate word. The table shows how this is accomplished. Assume that word 1 (which would be located directly above word 3) became garbled or lost, word 3, word 5, and the Orthoword are added by the Orthotronic Add instruction. As a result of the uniqueness of binary mathematics, this simple addition enables the machine to reconstruct the erroneous word into its original form. The same reasoning may be applied regardless of the number of channels involved.

Word 3	000001	001000	000111	010000	100111	010001	101001	100010	0100
Word 5	100101	010101	110110	010000	111000	100110	101001	100010	1001
Orthoword	000101	001100	010101	010101	101101	100111	010011	011011	1011
Total	100001	010001	100100	010101	110010	010000	010011	011011	0110
	J	A	M	E	S	space	C		

Errors in any two words within the same block, even though in different channels, are correctable if one occurs in an odd-numbered word and the other in an even-numbered word. Oxide flaking and dust particles on the magnetic tape contribute to the greatest percentage of errors in data processing equipment. Of the few which do crop up, the majority affect only one channel and can, therefore, be corrected automatically by the machine. In relatively infrequent instances, particles of dust or foreign matter may be large enough to affect two adjacent channels. The majority of these errors are correctable, since the words are arranged on the tape in a unique staggered fashion. In most cases, therefore, these particles will influence an odd and an even word within the same block or two odd or two even words in adjacent blocks. All of these situations are correctable. The correction procedure outlined above is initiated by the machine only when an error is detected. If the information is correct, the machine follows its regular routine since the Orthotronic Add instruction is not required. The weight count digit appended to the Orthoword is not the actual weight count of that word but rather the Orthosum of the weight of all companion words. Therefore if an information word is reconstructed using a defective Orthoword, its Orthocorrected weight count will not agree with its originally computed weight count. In practice, this may be checked by the Orthotronic Add instruction. This provides a means for double checking each correction. If the Orthocorrected information does not have a valid weight count, it obviously was regenerated using a defective Orthoword.

There are a few instances where the machine alters the procedure outlined above. If, by some remote possibility, errors occur in two odd-numbered words or in two even-numbered words within the same block, the programmer may select any of several alternatives. In many of these cases it will be found that after the alternatives have been tried, the error will have been eliminated. In those rare instances where none of these methods is effective, the computer will begin the regular detection subroutine. This eliminates any possibility of an inaccurate word being carried through the system.

Orthochannels are also generated within the Input Converter. The DATAmatic 1200 Card Input System is used to read punched card information and to convert it to a binary representation for writing on magnetic tape. Each punched card is converted to one 16-word record or blockette on tape: 14 words derived from the card, one word of identification and one control word. Two such records are written on each tape block. In addition, circuitry is now being added to the Input converter to include two Orthochannels, one for each blockette. Each blockette carries its Orthochannel until the card data is transferred into Central Machine memory and is confirmed. The contents of the blockettes may then be processed, and conveyed to the Output Buffer where the data is assembled for writing onto magnetic tape. When a Write instruction is given, a new Orthochannel is generated for each block.

DOCUMENT DATA PROCESSING SET, AN/GSQ-13(XW-1) - U.S. AIR FORCE - WASHINGTON, D.C.

The Document Data Processing Set is a general purpose computer especially designed for problems requiring a high degree of correlating ability. Specialized commands have been designed for data entry, data reorganization, and data look-up so as to facilitate decision making. The set is being used to control the dissemination of documents to organizations and individuals interested in specified subject areas. The internal memory file contains the set of customer requests against which the document coverage is compared.

The main memory is a magnetic drum, 16" in diameter, rotating at 1800 rpm. It has been designed for capacity up to 22,000 words of storage, each word consisting of ten alphanumeric characters. Information is recorded in channels each divided into 100 sectors. A word of information can be stored in any sector in any channel. Provision has been made for up to 220 channels for the total capacity of 22,000 words of storage.

Information is represented as fixed length words, each containing 60 bits. A single such word may be used to represent 10 characters of alphanumeric data, 15 characters of numeric data, or a command. The command word consists of: three decimal digits, which specify the operation, five which specify the address of the operand, and five which specify the address from which the next command is to be taken. Such a structure is frequently called a "one-and-one" address command.

Checking features are: Storage of an additional bit with each word to serve as a parity check. Checks to verify the reliability of the internal logical elements by checking the consistency of the counters, the timing circuitry, the instruction execution, and the state of decision elements. The operation of the input device is checked by a parity bit for each character input.

Programs have been prepared for controlling the Document Data Processing Set in the determination of groups or individuals interested in particular documents. Requests for information form the basic file against which incoming documents must be compared. These requests specify subject and area of interest together with other qualifying data (such as evaluation, type of copy desired, etc.) and the identification of the customer making the request. The requests are stored internally on the magnetic drum, one to each word. The capacity has been designed for storage of up to 20,000 requests.

A dissemination operation involves the following steps. The subject and area coverage of a document, which were previously punched into punched paper tape, form the input. The individual words must be grouped by the Document Data Processing Set into phrases of the same structure as the stored requests. Since several combinations of subjects and areas may be covered by the document, the phrases describing the coverage given by the document must be analyzed and all valid combinations searched against the file.

The file search commands have been designed so that generically coded requests will pick up all relevant documents concerned with sub-categories. Each valid subject-area coverage of the document is searched against the file of requests. The result will be the output of a list of requestors for the document and, if desired, the area of interest for each requestor.

The file handling commands have been designed to facilitate the addition of new requests to the file and the deletion of out-moded requests. Programs have been prepared for complete listings of the file of requests, in order by requestor identification. These can thus be screened for need to know, etc.

A library of sub-routines for other operations has been prepared. This can be expanded, and the machine applied to a number of other tasks such as: file indexing, item coding and translation, pattern recognition, etc.

The system has been in operation since July 1958 at the Headquarters, U. S. Air Force, and was manufactured by the Magnavox Research Laboratory, Los Angeles, California.

COMPUTING CENTERS

DATA REDUCTION LABORATORY - AIR PROVING GROUND CENTER - ELGIN AFB, FLORIDA

An IBM type 738 Magnetic Core Storage Unit with 32,768 words, was installed in the 704 system replacing the two 737's.

Elgin Air Force Base's Civilian Payroll accounting was mechanized for the 704. Now being used for confidence checking against the previous methods, the payroll program will start independent operation and actual check preparation with the last quarter of this year. This program is believed to be a first for payroll preparation in the Air Force on a 704 computer.

Bendix Computer Division has delivered a Telemetry reception, digital conversion and Univac Scientific Computer input system which is being acceptance tested. The equipment will permit quick, or even real time telemetry data reduction.

Further telemetry and magnetic tape data reduction facilities have been assembled into the system called TELEMAG, of which the Bendix equipment is a subsystem. This facility provides a broad and general capability for analog and digital data processing (see Digital Computer Newsletter, January 1958).

SWAC - UNIVERSITY OF CALIFORNIA - LOS ANGELES, CALIFORNIA

A magnetic core memory, utilizing RCA ferrite core plates, is under construction. A revision in assembly procedure as well as in internal arrangement of the plates allows modules of 16 words, each of 48 bits, to be constructed. Each module contains its own driving and sensing circuitry. Amplifiers and coding network are separately mounted. All circuitry is transistorized and on printed circuit boards. The modular method of assembly permits replacement of an individual plate if defects or malfunctions make this necessary.

The core memory will have a capacity of 256 words of 48 bits each. It is now planned to operate this memory in conjunction with the 256 word electrostatic memory to provide enhanced storage. Two logical control methods are being considered. Either the internal logic of the computer will be altered to permit independent addressing of either memory without increase of word length, or the word length will be increased and the four address logic left unchanged. No decision has been reached on this as yet.

Preliminary plans have been made for moving SWAC to new quarters in October 1959. Most of the wiring between the main sections of the computer will be replaced with modern cabling, and multi-prong plug and receptacle connections will replace the present soldered terminal boards. The core memory will be installed and tested before the move. The computer will be "off the air" for approximately 3 months. It is planned to install a new console at the new location, and design work on this project has begun.

The computer has been operated at somewhat lowered efficiency during the last few months. Some time has been assigned to wire tracing in preparation for the removal, and considerable time has been spent on a study of the arithmetic organ. Some experiments to determine faults in the design of the adder have led to circuit alterations which have improved the operation for this portion of SWAC. Further studies of undesirable side effects of the alterations are going on. It is expected that the arithmetic organ can be improved further.

The work on SWAC continues to be done by graduate research assistants and undergraduate technicians, all working part-time. The magnetic core memory is being constructed completely in our laboratories at Numerical Analysis Research. Techniques in printed circuitry construction and dip soldering are being developed. Valuable training in the field of practical shop work, as well as in logical design and theoretical research is being provided to these students.

AERODYNAMICS LABORATORY - DAVID TAYLOR MODEL BASIN - WASHINGTON 7, D. C.

The Aerodynamics Laboratory of the Navy's David Taylor Model Basin has added an Alwac III-E digital computer to its data processing systems. For several years an Alwac II has been used to process data from the Laboratory's Transonic Wind Tunnel. Now the output of data from two Subsonic Wind Tunnels is automatically put on punched paper tape. Either 6 or 12 channels of information can be accommodated, together with several channels of semi-automatic identification data. The tapes are then fed to the Alwac III-E computer, which furnishes tabulated corrected data, ready for analysis and reporting.

AEC COMPUTING AND APPLIED MATHEMATICS CENTER -
NEW YORK UNIVERSITY - NEW YORK, N. Y.

UNIVAC I System. Recent machine modifications include the following:

1. The installation of a manually operated system to facilitate the assignment of any computer number to any servo. Positioning of an eleven-position switch located at the servo which simultaneously selects one of ten computer numbers, indicates the one selected by lighting an enditron, and provides a warning if another servo has been assigned the same computer number.
2. An addition to the N.Y.U. instruction code based upon a previously reported modification (Digital Computer Newsletter, October 1957) of the Univac Control Counter. This instruction, known as R1, may be either programmed or manually selected. Although of restricted usefulness, its effectiveness in aiding debugging of new codes will save much computing time.
3. A "Last Read Indicator" has been installed. The last read indicator performs the function of indicating, at supervisory control, the last servo which was moved in a read operation. The device is useful for the following reasons:
 - a. Allows operator to rock a tape without identifying the servo.
 - b. Records the last servo read in case of bad I tank to memory transfer, which allows the saving of the program in many cases.
 - c. The indicator allows a programmer to follow his tape movements in debugging.

Since the indicator is separate from the machine operation, no machine down time is necessary during the installation other than the connections to the backboards.

Machine time is readily available at present on the UNIVAC I. There is no charge to AEC contractors, and contractors of other government agencies can be allotted time at established hourly rates.

Inquiries should be addressed to Professor R. D. Richtmyer, Director, AEC Computing and Applied Mathematics Center, 4 Washington Place, New York 3, New York.

MATHEMATICS DEPARTMENT - U.S. NAVAL ORDNANCE LABORATORY,
WHITE OAK - SILVER SPRING, MARYLAND

NOL expects to take delivery of an IBM 704 in January 1959. This computer will replace the two IBM 650's presently in operation at the Laboratory.

The former Applied Mathematics Division at the Naval Ordnance Laboratory has recently been elevated to departmental status. It is now known as the Mathematics Department and contains two new Divisions, the Mathematical Analysis Division and the Mechanized Computations Division.

NAVAL ORDNANCE COMPUTATION CENTER -
U. S. NAVAL PROVING GROUND -
DAHLGREN, VIRGINIA

Hardware is now being assembled for the Universal Data Transcriber (UDT), scheduled for completion early in 1959. Logical design of the UDT is being tested by a simulation routine on the NORC. Another NORC routine is being used to select, among several wiring layouts, the one resulting in minimum wire lengths and absence of excessive loading on individual logic circuits. Input-output media initially provided for will be NORC tape, punched cards, and punched tape; others will be added as needed.

Another conversion device has been completed and tested, its use being needed earlier than the expected completion of the UDT. This special purpose device accepts three-decimal-digit-and-sign samples from an analog-to-digital converter at the rate of 6,000 samples per second, and writes the samples on NORC tape.

A contract has been awarded to Daystrom Instrument for a 20,000 word ferrite core memory with eight microsecond cycle, to replace the present 2,000 word Williams tube memory of the NORC. Delivery is due in mid-1959.

The Aiken Dahlgren Electronic Calculator (ADEC) has been dismantled after being idle for some months. Completed in early 1950 by the Harvard University Computation Laboratory under Professor Howard Aiken, the ADEC was the pioneer among large magnetic drum calculators.

DIGITAL COMPUTATION BRANCH (WCLJU) - WRIGHT AIR
DEVELOPMENT CENTER - WRIGHT-PATTERSON
AIR FORCE BASE, OHIO

The Scientific Computation Facility of the Wright Air Development Center now uses two Univac Scientifics to solve the engineering problems that arise in the Center. The first Model 1103 with magnetic core storage was installed January 1956 and has been in three shift operation since July 1956. For the first seven months of 1958, average power-on time (excluding two hours of preventive maintenance per day) was 468.9 hours per month. For the same period emergency maintenance averaged 3.9 hours per month and reruns, due to computer malfunction, averaged 4.1 hours per month. Thus the computer was available 460.9 hours per month, an efficiency of 98.3% of power-on time.

The newer Model 1103A was installed May 1958. One shift operation has been used since 2 June 1958 with a second shift scheduled for January 1959. The average efficiency was 97.9% of power-on time for June and July. The equipment includes 12,288 words of core storage, floating point feature, 8 Uniservos, high speed printer (on or off-line), Bull Reproducer, etc.

The OARAC Computer, built in 1952 by the General Electric Company, is presently undergoing extensive modifications, including a 10,000 word core storage. It will be used in the future as a research computer under an "open-shop" operation by the Aeronautical Research Laboratory.

COMPUTERS, OVERSEAS

GAMMA 60 - COMPAGNIE DES MACHINES BULL - PARIS, FRANCE

Note.—The following informal review of the GAMMA 60 characteristics was contributed by Mr. Harry Hayman, U. S. Navy Bureau of Ships (Code 687E), Washington 25, D. C. Additional information concerning the machine may be obtained from the Compagnie des Machines Bull, 94, Avenue Gambetta, Paris, France.

The GAMMA 60 computer manufactured by the Bull Company, Paris, France is a high-speed solid state computer designed for data processing. It is based on the concept that the memory is the most expensive portion of the computer and therefore should be kept busy all the time. The memory is used as a buffer between all units.

Before proceeding, a discussion of the basic word length is necessary. The basic word is 24 bits, however, this is not a true word, but called a CATENA. The various units can operate on variable CATENA lengths, with the exception of the arithmetic unit which always operates on two CATENAs. To conserve memory space the arithmetic unit operates on a four bit binary

coded decimal digit; the program word, which may be one, two, or three CATENAs long is in binary; and the input-output and other units can operate on a six bit binary coded alphanumeric.

The individual units within the system are:

- | | |
|--------------------|-----------------------|
| 1. Arithmetic Unit | 6. Card Reader Unit |
| 2. Logical Unit | 7. Paper Tape Unit |
| 3. Compare Unit | 8. Magnetic Tape Unit |
| 4. Translate Unit | 9. Magnetic Drum Unit |
| 5. Printer Unit | 10. Card Punch Unit |

All of the individual units communicate directly with the core storage. They cannot communicate with each other except through the program distributor. Each unit is a little computer within itself. Each unit besides performing its basic function consists of a simple adder (to add or subtract one from its current address register), three current address registers (instruction counters), programming register, and one CATENA input and output buffer.

To provide the central control for these various units there is a program distributor, which receives from all units requests for instructions; and a transfer distributor which receives, from all units, requests for data. The magnetic core memory has an 11 microsecond access time for each CATENA. Therefore not all units can refer to the memory simultaneously and the program distributor has priority circuits to control the access to memory. Because the slowest units are mechanical in nature and difficult to stop they have the highest priority to memory, and the fastest units, which are electronic and can easily be stopped, have the lowest priority to memory. Priority is as follows:

- | | |
|----------------|------------------|
| 1. Card Reader | 5. Magnetic Tape |
| 2. Card Punch | 6. Arithmetic |
| 3. Printer | 7. Logical |
| 4. Drums | 8. Compare |

Thus if we consider the arithmetic unit, it will start with a C type instruction which will cut it into operation. If the program it is working on is in location 101 it will start at location 101 and continue on until it reaches the next C or cut type instruction. The arithmetic unit then looks at its next current address register, which tells it where the next series of instructions for the arithmetic unit begins. This information has previously been supplied by the program distributor. After each operation every unit sends one CATENA of information back to the program distributor, which supplies error, transfer, and other information to the program distributor.

In order to operate units simultaneously, there is a conditional transfer instruction which is an "and" type operation and can call for cut instructions to two different units. As many of these transfers as are necessary to put the desired units into operation may be used. There is also a regrouping conditional transfer which will prevent the transfer until each of the units have reported that their work has been completed.

Other features of the computer are:

1. Transistor, diode, and magnetic core logic.
2. No off-line equipment.
3. Variable CATENA operation.
4. One, two, and three address instructions.
5. Each CATENA individually addressed. 4096 to 32,768 CATENA memory.
6. 4 alphanumerics or 6 numerics per CATENA.
7. Indirect addressing may continue indefinitely.

8. Two and three address compare instructions in many forms and in variable CATENA word length.

9. 11 millisecond average access time for the drum. 44 microseconds transfer time per CATENA for drum. 32,768 CATENA on each drum.

10. 11 microseconds for a comparison.

11. Arithmetic speeds (decimal, floating point):

Addition	100 microseconds av.
Multiplication	300 " "
Division	600 " "

All arithmetic operations 2 CATENAs in length.

12. \$1.5 million purchase price for basic system with 4096 CATENA memory.

13. Engineering prototype now in production to be completed by April 1959. 1st delivery of commercial model scheduled for October 1959.

14. No plugboards provided on input-output unit. All editing done by translate unit with special instructions using three address instruction.

- A. Address of information to be edited
- B. Format address
- C. Address to store result

15. Logical operations 20 microseconds plus access time.

16. Uses about 15,000 U.S. transistors for the entire computer, General Ceramic cores, and Electrodata or Ampex tape units.

17. 120 character line printer, 300 lines/minute.

18. Checking:

A. Three extra bits per CATENA which give a remainder when divided by seven. During addition divides the addend, augend, and total by seven, and compares the sum of the remainders with the remainder of the sum.

Remainders	
31	3
+43	+1
74	4

B. Card reader reads two or three times. Compares first and second reading. If necessary makes third reading and selects correct reading of first two.

- C. Card punch reads after punch.
- D. Echo check on print.
- E. Reads paper tape after punch.
- F. Reads paper tape twice.
- G. Compares memory address with that actually requested.

19. Reads 300 cards/minute.

Comparison of GAMMA 60 with IBM 705

	GAMMA 60	IBM 705
Add	100 microseconds	119
Multiply	300 " "	1819
Input (120 digits - Memory time only)	242 " "	1141
High speed memory access	11 (4 alphanumeric)	9 (1 alphanumeric)
Arithmetic	Fixed and floating	Fixed

Memory Access Time (Microseconds)

GAMMA 60 IBM 705		
6 Decimals	11	54
4 Alphanumeric	11	36
Single address instruction	11	45

In comparing the two computers it should be remembered that if memory is kept busy on the 60, several operations may be performed simultaneously, whereas on the 705 only input-output and one computer operation may be performed simultaneously. Also one memory reference in the 60 is the equivalent of 4 alphanumeric or 6 decimal references in the 705.

MERCURY - FERRANTI, LTD. - MANCHESTER, ENGLAND

Ferranti Mercury High Speed Electronic Computers are now in use at:

U. K. Atomic Energy Authority, Harwell.
French Atomic Energy Authority, Paris.
Norwegian Defence Research Establishment, Oslo.

A fourth machine for the Council of European Nuclear Research recently completed its performance tests and was installed at the Council's headquarters in Geneva before the September Exhibition.

Altogether seven Mercury Computers will be used in the Nuclear Field. The major part of the computing work on Atomic Physics in Europe during the next few years will be done on these machines. A system has been set up for exchanging information among all users so that each user benefits by the accumulated experience of all the others.

An autocode has also been written for the machine which simplifies the preparation of problems and shortens the total time necessary to solve them. This makes it possible for Nuclear engineers to carry out their own calculations on it. These are essentially smaller than those met with by the Nuclear Physicists and more akin to those encountered in general engineering.

Mercury was introduced in August 1957, and can solve problems up to fifty times faster than any computer made in Western Europe. For three years Ferranti employed the largest team of Electronic Computer Research Personnel in the United Kingdom developing the machine. In the U.S.A. the Ferranti Electric, Inc., 30 Rockefeller Plaza, New York 25, New York, represents Ferranti, Ltd.

HIGH SPEED PRINTER - POWERS-SAMAS ACCOUNTING MACHINES, LTD. - LONDON, ENGLAND

The Samastronic Output Printer, for use with Electronic Computers, Magnetic Tape Control Units, and such like devices, employs a unique method of printing. Each individual character is formed by traversing a single stylus some 15 times across the width of one character above the printing paper. As the paper moves forward at a uniform speed, 140 styluses are continuously oscillated thus each stylus produces a scanning effect in much the same manner as the spot on a television screen scans the picture area.

The actual print is produced by pulsing the styluses on to an inked ribbon or carbon paper at appropriate times during the scanning cycle. The dots caused by pulsing the styluses can be produced at any point on the scan to form solid, distinct printed characters.

The machine has a total printing capacity of up to 42,000 characters a minute. This is achieved by mounting the 140 styluses, side by side in a single oscillating bar, thus enabling up to 140 characters to be printed in one line at a speed of 5 lines per second. Printing can be accommodated on most existing forms, eliminating the need for designing special stationery in many instances.

Fifty different pulse trains contained on a Character Disc Assembly in the Printer provide a repertoire of 50 characters. Printing format is determined by interchangeable connection units. Different formats may be selected by control signals for each line of print.

Two stationery feeding carriages are provided permitting two webs of continuous marginally-punched forms to be fed independently. Wide flexibility in stationery feeding programs is provided by automatically-compensated long-feeding facilities which are built into the machine.

A model has been displayed by Ferranti Electric, Inc., 95 Madison Ave., Hempstead, N. Y.

COMPONENTS

AUTOMATIC MULTIPLE PROGRAMMER - BUREAU OF THE CENSUS - WASHINGTON, D. C.

The Maintenance and Development Branch, Machine Tabulation Division, Bureau of the Census, has developed and is experimenting with an Automatic Multiple Programmer attached to an IBM 027 Keypunch Machine. This device permits the punching of six different card forms and changes the card form automatically on ejection of a card by the punch machine. A counter is provided which will accumulate a tally of the number of cards punched, and punch the total into the last card of the record automatically.

The console of the Programmer provides for manual overriding of the automatic advance feature to allow selection and repetition of any program. The card count is displayed on the console at all times, and there are indicator lights showing which program is in use at any time.

Programs are stored in printed circuit boards. Each program requires two circuit boards. The process on which the Programmer is being tested requires six programs. This number can easily be expanded. The device can also be connected to the standard Type 024 or 026 Keypunch machines.

The key punching of a complete record at one time has many advantages. The problem of work flow and accompanying controls is reduced drastically. More of the data common to all cards for a record can be automatically duplicated. The cards produced from the record are together at the time of their creation, thus eliminating merging operations on more expensive punch card equipment.

Optimum use of punch cards as an initial recording media makes mandatory the use of variable length fields. Therefore different card formats are required for different portions of the record. The Automatic Multiple Programmer provides the facility to punch six different formats consecutively and makes possible the punching of a complete record at one time by one operator.

In the past the processing, by an electronic computer, of multiple card records, where the number of cards varies, has been complicated by the inability to determine completeness of the data. There was no positive assurance that all cards for the record had been recorded consecutively on magnetic tape. Yet the capabilities of a computer can be employed to a much greater extent if a complete record is processed as a unit. The automatic recording, of the number of cards punched for a record, in the last card of the record, provides a control medium for determination of its completeness when processing on a computer. In fact, with this attachment, punch cards can now assume some of the advantages of paper tape in the continuous recording of related data.

METALLIC TAPE CLEANER - DIGITRONICS CORP. - ALBERTSON, N.Y.

The Dykor Metallic Tape Cleaner has been designed to solve the problem of dirt and grime accumulation on metallic tape. Presence of foreign matter results in reading gaps as well as excessive machine wear. The operation of the cleaner is semi-automatic and results in completely cleaning and relubricating an entire reel of tape in a matter of minutes. At the completion of the process, the tape is rewound and ready for immediate use. No data is destroyed.

The Dykor Cleaner is a compact portable floor model mounted on casters. It is 21" x 18" and approximately desk height. Construction is rugged and designed for continuous use. This completely self-contained unit could add years to the life of both the metallic tape and the tape handler.

ALWAC UNIVERSAL TESTER - EL-TRONICS, INC. - HAWTHORNE, CALIFORNIA

To further increase the high reliability of the ALWAC III-E Electronic Data Processing System (national average: above 90% uptime), the ALWAC Computer Division has announced a new plug-in unit tester. It is designed to be universal in scope and will accommodate all possible circuit configurations currently employed or proposed for the ALWAC Computer System. The heart of the unit is a printed circuit grid card which permits 32^{33} combinations. The mode variation increases the number of combinations by 2^5 , load combinations by a factor of 2^4 , and power supply connections by 2^7 . Other parameters such as signal rise-fall-time extensions, special tests, power supply ranges, and test signal levels increase the number of combinations almost infinitely.

A grid card is required for each circuit type to be tested and this card, when inserted, will determine the mode of test. A major advantage of the Universal Tester is the simplicity of operation. Instructions as to the set-up for only six manually operated switches are made available on each grid card.

It is anticipated that the Tester will enable more efficient computer operations considering the decrease in training costs of maintenance personnel, as well as a decrease in time for maintenance sessions.

HIGH SPEED TAPEREADER - ELECTRODATA DIV. - PASADENA, CALIF.

A perforated paper tape reader which operates at 1,000 characters/second has been announced by the Burroughs Corporation's ElectroData Division. The photoreader will stop on a single stop-character in a little more than a microsecond and will read the next character within five milliseconds of re-initiation of the read operation.

Although the unit is designed for use with their 220 electronic data processing system, it may be adapted to any equipment. Delivery is currently quoted as four months.

Some features are: Automatic rewind and end-of-tape sensing. Rapid, simple "straight-line" tape loading. Automatic reel braking and servo shutoff system to prevent tape damage and consequent loss of data in the event of power failure, tape breakage, or other malfunction.

NEURON COUNTER - DATA INSTRUMENTS DIV., TELECOMPUTING CORP. - NORTH HOLLYWOOD, CALIFORNIA

Telecomputing's Data Instruments Division has a new bi-directional counter which is a rapid-follow function digital indicator. Known as the NEURON counter, it can be used to indicate the position of almost any discrete variable such as valve opening, shaft position, angle of magnetic tape position. It can also be used to store in-out information which is necessary for inventory control bi-directional flow, liquid quantity and flow indication, or batch tabulation. Special units, for example, digital clocks are available.

The standard counting rate of the counter is 0 to 40 counts per second. Separate add and subtract motors allow random input pulses. Reset can be manual by a single-stroke push bar or electrical by a remote switch pulse. The unique drive prevents double-indexing arising from shock vibration and over-voltage. The digital readout to five decades can be both electrical and visual.

The electrical readout feature consists of an etched 10-point switch and circuit combination which makes each point on the switch externally available. A 10-point epoxy-glass etched switch deck is mounted adjacent to each counter wheel and projects through the bottom of the counter case for electrical connection. An insulated rotor attaches to each counter wheel position. Each rotor connection is brought out through a slip ring on its mating switch deck. The life of a counter is in excess of 300 million counts.

CORE STORAGE - TELEMETER MAGNETICS, INC. -
LOS ANGELES, CALIF.

Telemeter Magnetics new magnetic core storage buffer, type 1092-BQ8A, operates at 100-kc rate and stores up to 1092 eight-bit characters. The prime application area for this unit is in synchronizing two digital data systems which operate at different speeds. For example: communication between a tape unit and a telemetering system; between an analog-to-digital converter and a computer tape unit; or between two units of different design. The buffer is also a necessary element in systems for converting from one format to another as from IBM magnetic tape code to UNIVAC code. The unit is available from stock. Functional features include:

The buffer is supplied as an integral unit in a standard 19 inch relay rack. All connections are made by means of plug connectors. Adequate cooling is provided by ambient air.

A conveniently located "manual clear" control clears information stored in the buffer unit and resets it to an initial fixed address. Connections are incorporated for easy installation of a remote clear push-button or switch. The complete clear and reset operation is executed in approximately 50 milliseconds.

Interlaced load and unload permits any random pattern of load and unload signals at rates up to 100,000 signals per second.

The buffer incorporates signal generating circuits for checking the operation independent of external equipment. In addition, manual controls permit marginal operation to locate weak or intermittent signals.

SPEEDREADER 2000 - UPTIME CORP. - RAWLINGS, WYOMING

The prototype model of the SPEEDREADER 2000 punch card input system has been in full operation at the factory for more than six months, following an extensive period of thorough testing.

The unit handles and senses cards reliably at a rate of 2000 cards per minute. The prototype reads 80-column cards; production models will be available to read 80- or 90-column cards.

Card sensing and timing is done photoelectronically. No mechanical elements are used in timing. A card is sensed row by row at an 80- or 90-column sensing station by 80 or 90 photodiodes. Row read-time is established by the leading edge of the card striking each of 12 photodiodes mounted vertically in the center of the card path.

Card-sensing registration is completely reliable, and the angular deviation from the horizontal encountered during card travel does not cause reading of an adjacent column rather than the correct one.

With this new equipment, high-speed data processing systems can use card data at speeds more nearly compatible with that of the central computer. The reading rate can increase the capabilities of conventional tabulating installations, and the operation of card-to-magnetic-tape conversion units can be speeded up.

The 2000 is available with or without electronic circuitry (vacuum-tube or transistorized) for large-scale or medium-sized data processing systems or for electro-mechanical accounting systems.

MISCELLANEOUS

INTERDISCIPLINARY CONFERENCE ON SELF-ORGANIZING SYSTEMS - CHICAGO, ILLINOIS

An Interdisciplinary Conference on Self-Organizing Systems will be held on May 5 and 6, 1959, in Chicago, Illinois. The conference is being sponsored by the Office of Naval Research, Information Systems Branch, with the assistance of the Armour Research Foundation of the Illinois Institute of Technology. The major function of this conference is to bring together research workers in the fields of the Biological, Mathematical, Physical, Psychological, and Social Sciences who have actively considered the development and growth of Systems capable of spontaneous classification of their environments. Emphasis will be placed primarily on non-biological mechanisms which exhibit characteristics of organization and growth, of thought and learning, of information and communication—those characteristics which are normally attributed to intelligent organisms.

Interested individuals may obtain further information and a preliminary program, when available, by writing to Mr. Scott Cameron, ICSOS Conference Secretary, Armour Research Foundation, 10 West 35th Street, Chicago, Illinois.

CONTRIBUTIONS FOR DIGITAL COMPUTER NEWSLETTER

The Office of Naval Research welcomes contributions to the NEWSLETTER. Your contributions will assist in improving the contents of this newsletter, and in making it an even better medium of exchange of information, between government laboratories, academic institutions, and industry. It is hoped that the readers will participate to an even greater extent than in the past in transmitting technical material and suggestions to this Office for future issues. Because of limited time and personnel, it is often impossible for the editor to acknowledge individually all material which has been sent to this Office for publication.

The NEWSLETTER is published four times a year on the first of January, April, July, and October, and material should be in the hands of the editor at least one month before the publication date in order to be included in that issue.

The NEWSLETTER is circulated to all interested military and government agencies, and the contractors of the Federal Government. In addition, it is being reprinted in the Communications of the Association for Computing Machinery.

Communications should be addressed to:

GORDON D. GOLDSTEIN, Editor
Digital Computer Newsletter
Information Systems Branch
Office of Naval Research
Washington 25, D. C.

Numerical
Analysts
•
Digital
Computer
Programmers



The Jet Propulsion Laboratory is currently expanding its digital computer facility to include an IBM-704. The digital computer facility is used to provide numerical solutions to the many problems encountered in space travel projects and missile research and development programs.

Many of the engineering problems encountered require the development of new mathematical techniques in order to use the digital computer in determining numerical solutions. Positions now exist for persons to carry on research projects in numerical analysis and to apply advanced numerical techniques to engineering problems. A Ph.D. in Mathematics or an M.S. with experience and U.S. Citizenship are required.

The expanded digital computer operations have provided several professional openings for experienced programmers with a background in mathematics and standard numerical techniques. A B.S. in Mathematics or Physics is required with experience in digital computer programming. Excellent opportunities for professional growth and recognition exist in a rapidly growing group.

JET PROPULSION LABORATORY
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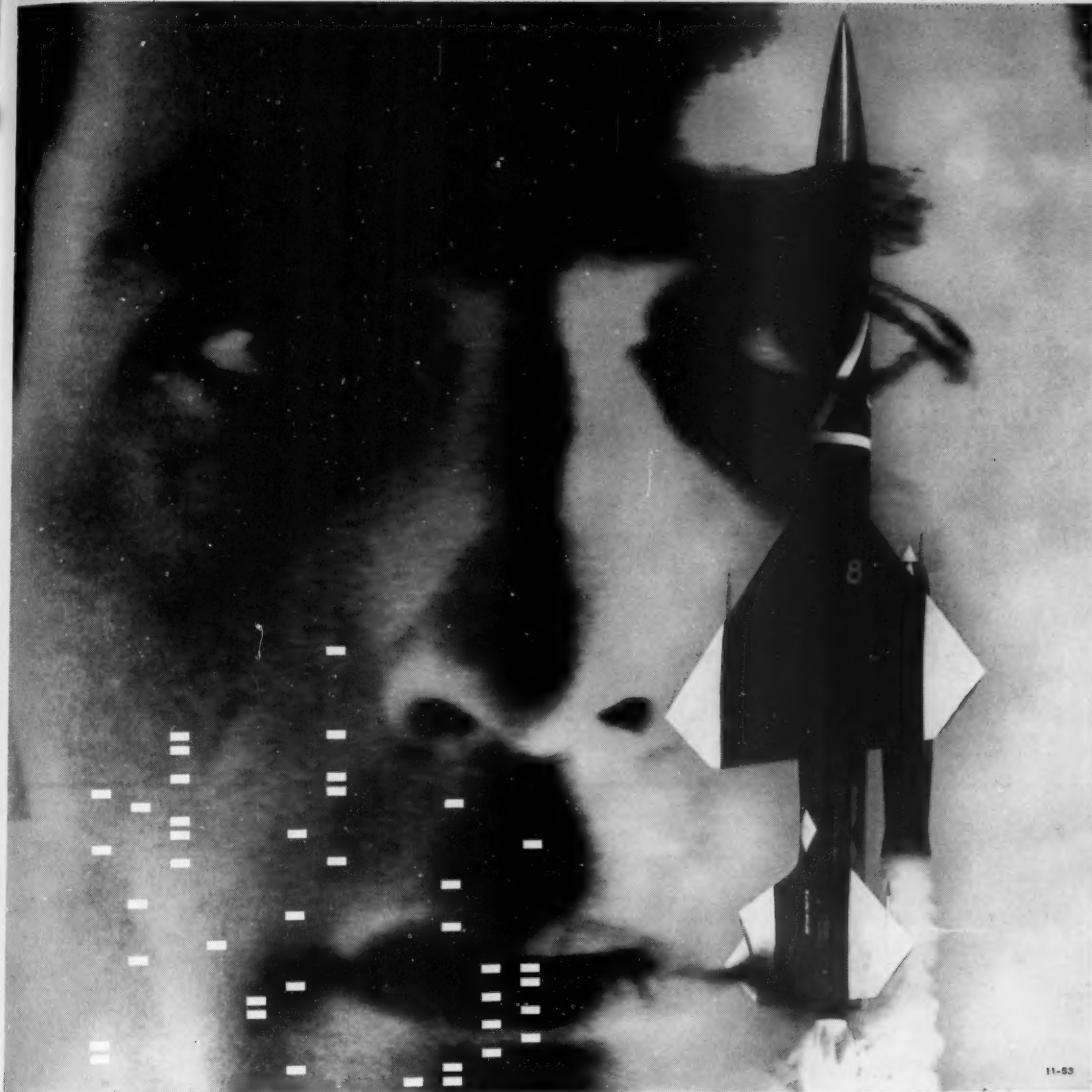
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11-53

Man-Machine Relationships:



A New Field for Computer Programmers

A new field for Computer Programmers has arisen from System Development Corporation's work on relationships of men and complex machine systems.

The work involves two major projects: 1 *creating and conducting large-scale training programs in present and planned air defense systems*, and 2 *operational computer programming for SAGE*. Each project requires intensive programming efforts in areas of real-time analysis and data reduction, using the most advanced computing equipment—704, 709 and SAGE computers.

The ultimate goal of Computer Programmers in each project is to attain the most effective interaction between men and machines and maximum utilization of those machines. They join with Operations Research Specialists, Engineers, and Behavioral Scientists to achieve this objective.

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The close interrelationship of these two major projects, the wide range of specialists involved in them, and the dominating influence of man-machine relationships makes SDC's work, in effect, a new field for Computer Programmers.

The expanding scope and importance of SDC's work has created a number of positions for experienced Computer Programmers possessing strong mathematical backgrounds and a high level of ability. Inquiries are invited. Address: R. W. Frost, 2446 Colorado Avenue, Santa Monica, California, or phone collect at EXbrook 3-9411 in Santa Monica.



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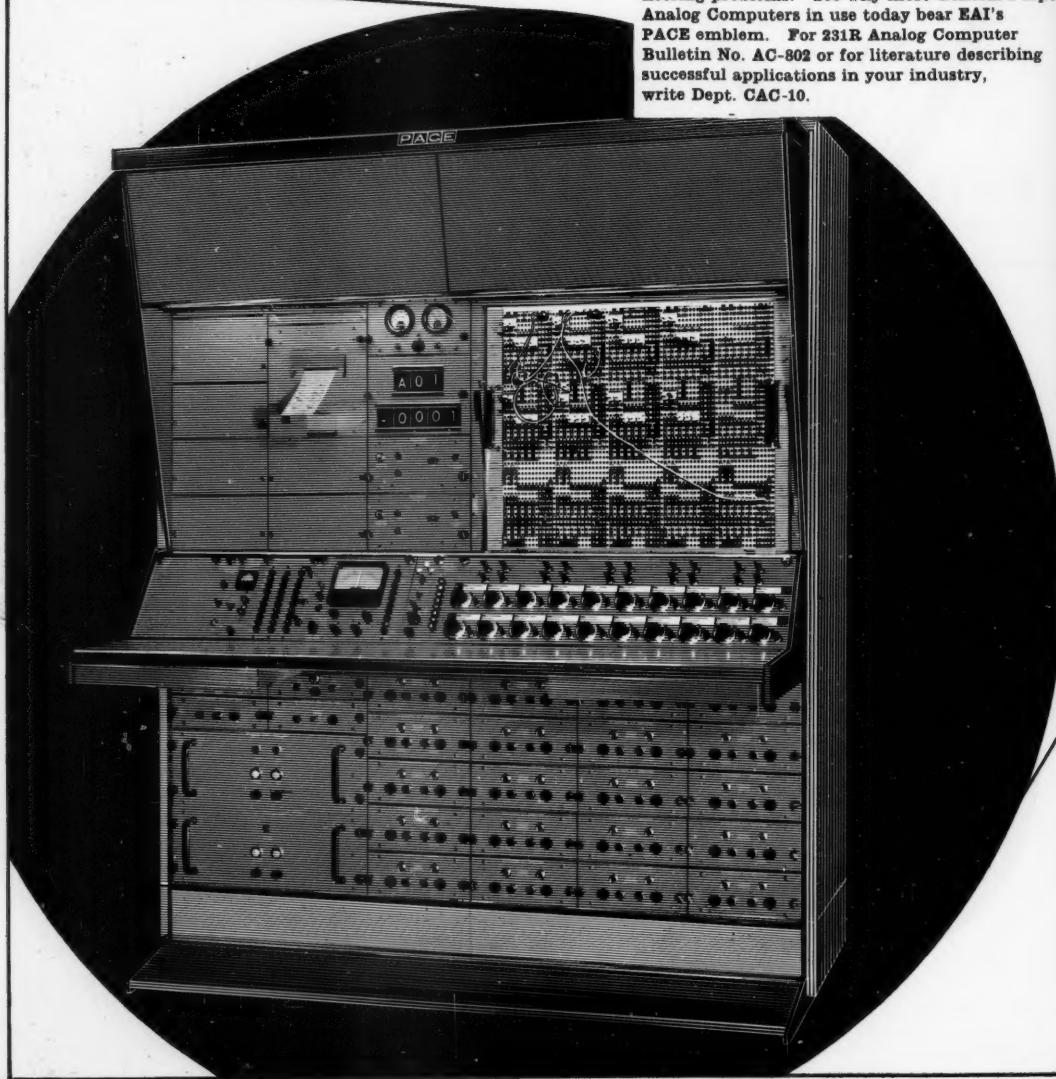


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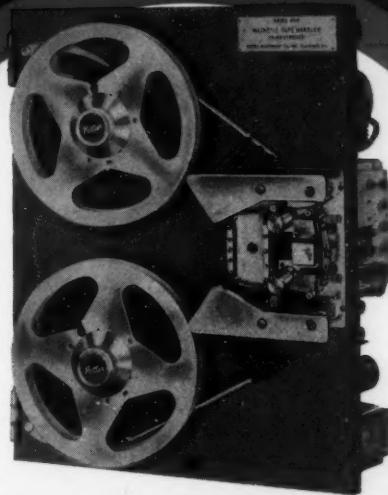
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For a personal interview, communicate with Mr. D. D. Brodhead.



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